PCB 101:

How Printed Circuit Boards are Made

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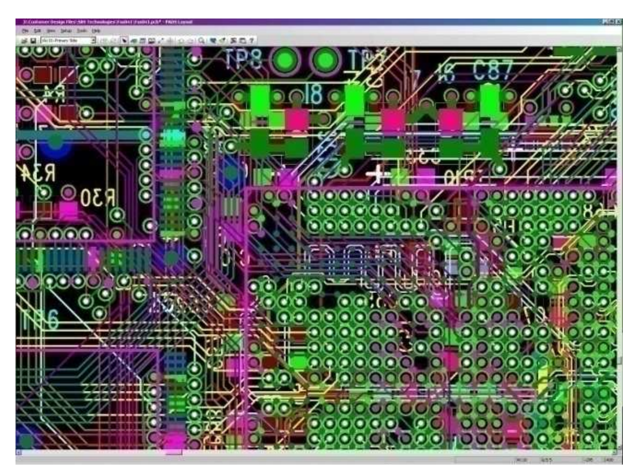
Midwest Region

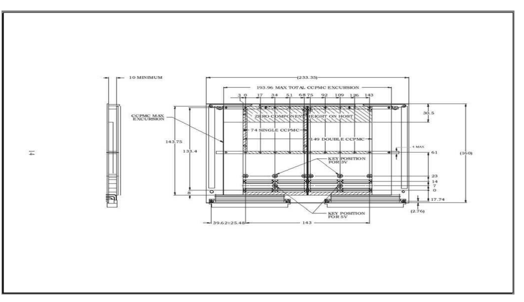
Tooling

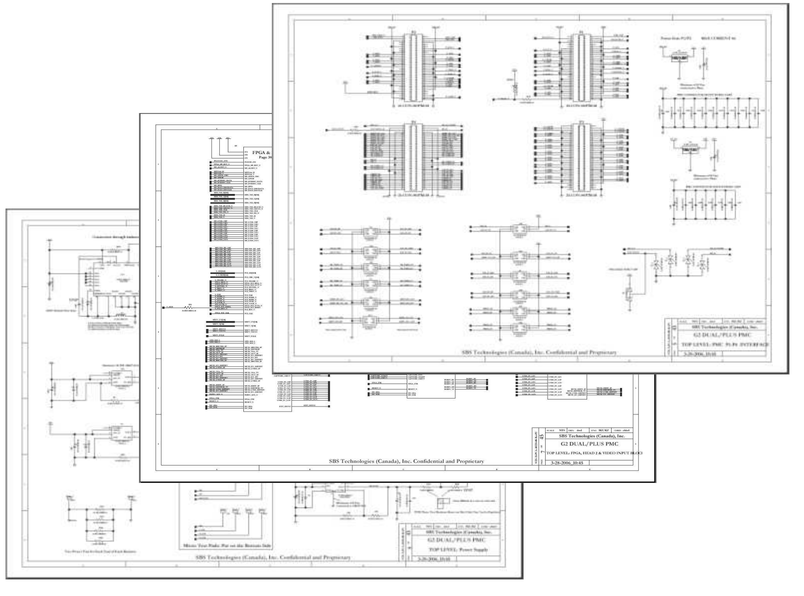
PRE-PRODUCTION ENGINEERING (Tooling)

Design Data Package

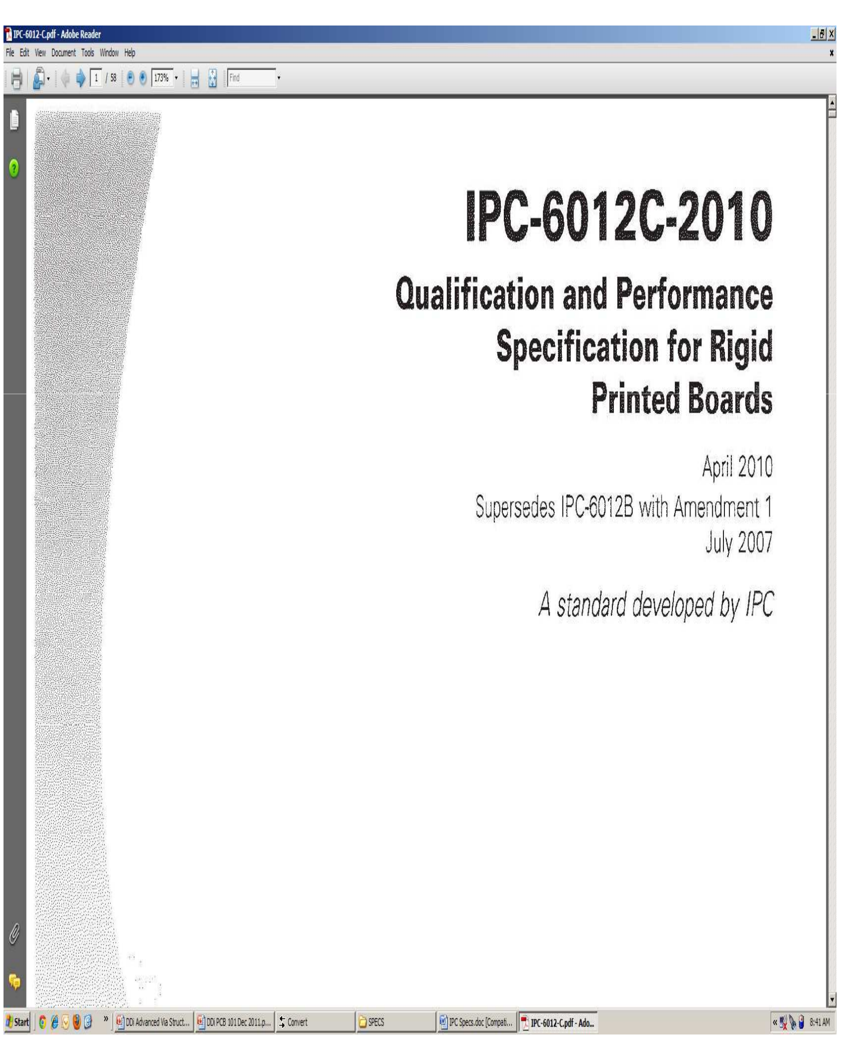
- CAD Data (ODB++ or Gerber 274x format)
- Independent Net List File (IPC-D-356)
- Fabrication Drawings
  - *Mechanical Dimensions*
  - *Build Requirements (materials, tolerances, surface finish, etc.)*







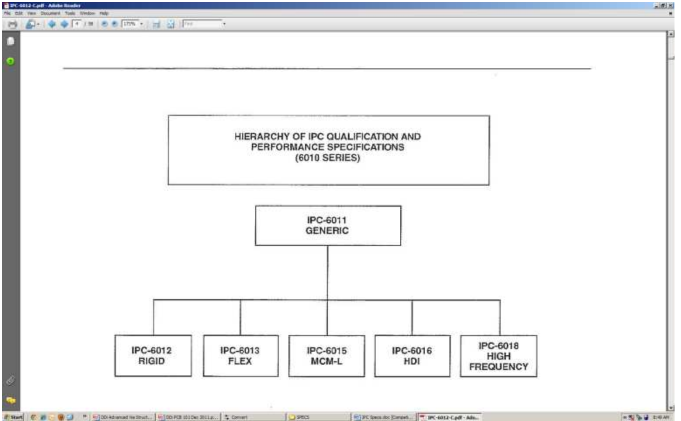
INDUSTRY STANDARDS (SPECIFICATIONS)



IPC

(Assoc. Connecting Electronics Industries)

- IPC-6012C is main build spec
  - *Classes (1, 2, 3)*
  - *Default reference specs*
- Other series include Design (IPC-2221), Materials (IPC-4101), Test Methods (IPC-652), etc.



PRE-PRODUCTION ENGINEERING (Tooling)

Methods Engineering

- Material Stackup
- Impedance Modeling
- Floor Travelers

Coretec Stackup Report

CORETEC

Customer: Example 2
Part No.:
Part Rev:
Facility: Toronto

Job:
Revision: 1
Engr: pcooke
Date: 06/01/2006

Layer	Thickness (Inch)	Stackup Picture	Family	Description	Type
M-1	0.0005		Probimer	Probimer 77	
L-1	0.0006		HTE6P	1/2oz	SIGNAL
	0.0062		370H		
L-2	0.0006		HTE6P	1/2oz	SIGNAL
	0.0052		370H		
L-3	0.0006		RTF5P	1/2oz	SIGNAL
	0.0041		370H		
L-4	0.0006		RTF5P	1/2oz	POWER_GROUND
	0.0061		370H		
L-5	0.0006		RTF5P	1/2oz	SIGNAL
	0.0060		370H		
L-6	0.0006		RTF5P	1/2oz	SIGNAL
	0.0038		370H		
L-7	0.0006		HTE6P	1/2oz	POWER_GROUND
	0.0061		370H		
L-8	0.0006		RTF5P	1/2oz	SIGNAL
	0.0050		370H		
L-9	0.0006		RTF5P	1/2oz	POWER_GROUND
	0.0062		370H		
L-10	0.0006		HTE6P	1/2oz	POWER_GROUND
	0.0038		370H		
L-11	0.0006		RTF5P	1/2oz	SIGNAL
	0.0060		370H		
L-12	0.0006		RTF5P	1/2oz	SIGNAL
	0.0061		370H		
L-13	0.0006		RTF5P	1/2oz	POWER_GROUND
	0.0041		370H		
L-14	0.0006		RTF5P	1/2oz	SIGNAL
	0.0052		370H		
L-15	0.0006		HTE6P	1/2oz	SIGNAL
	0.0062		370H		
L-16	0.0006		HTE6P	1/2oz	SIGNAL
M-2	0.0005		Probimer	Probimer 77	

Coretec Stackup Report

CORETEC

Customer: Example
Part No.: Stackup_0.090"
Part Rev:
Facility: Toronto

Job:
Revision: 2
Engr: pcooke
Date: 06/01/2006

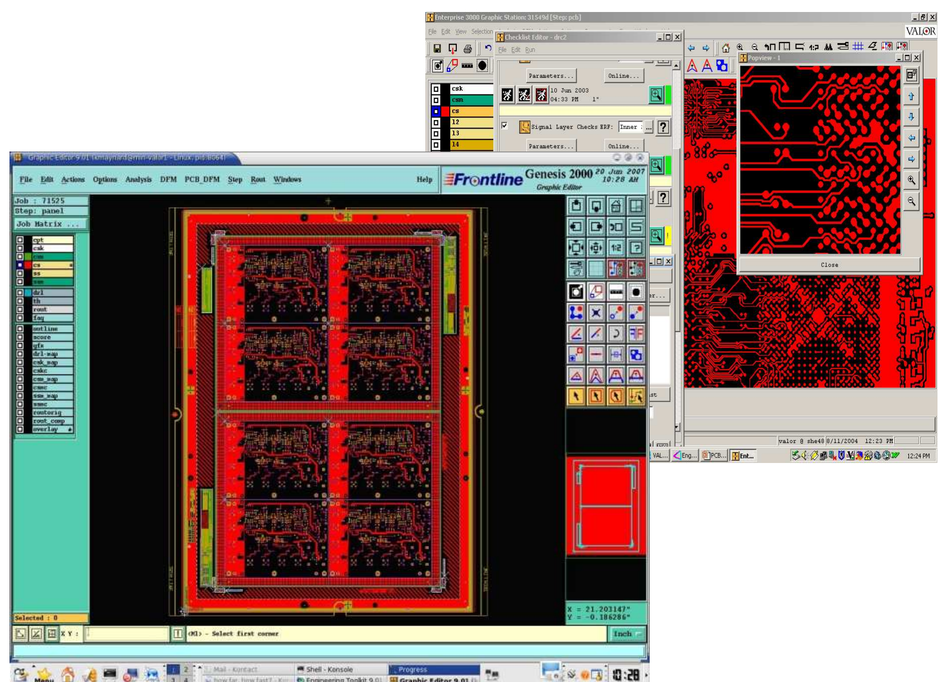
Requirements Information in Inch

Top Layer	Bottom Layer	Required Thickness	Tol +	Tol -	Calculated Thickness
Mask Top		0.0005			0.0005
Mask Bottom		0.0005			0.0005
Mask Top over Laminate		0.0007			0.0007
Mask Bottom over Laminate		0.0007			0.0007
Incl. Mask		0.0910	0.0070	0.0070	0.0888
Incl. Mask over Laminate		0.0874	0.0070	0.0070	0.0852
Incl. Plating		0.0900	0.0070	0.0070	0.0878
After Lamination		0.0872	0.0070	0.0070	0.0850
Over Laminate		0.0860	0.0070	0.0070	0.0838

Comments

Expanded Impedance Constraint Information

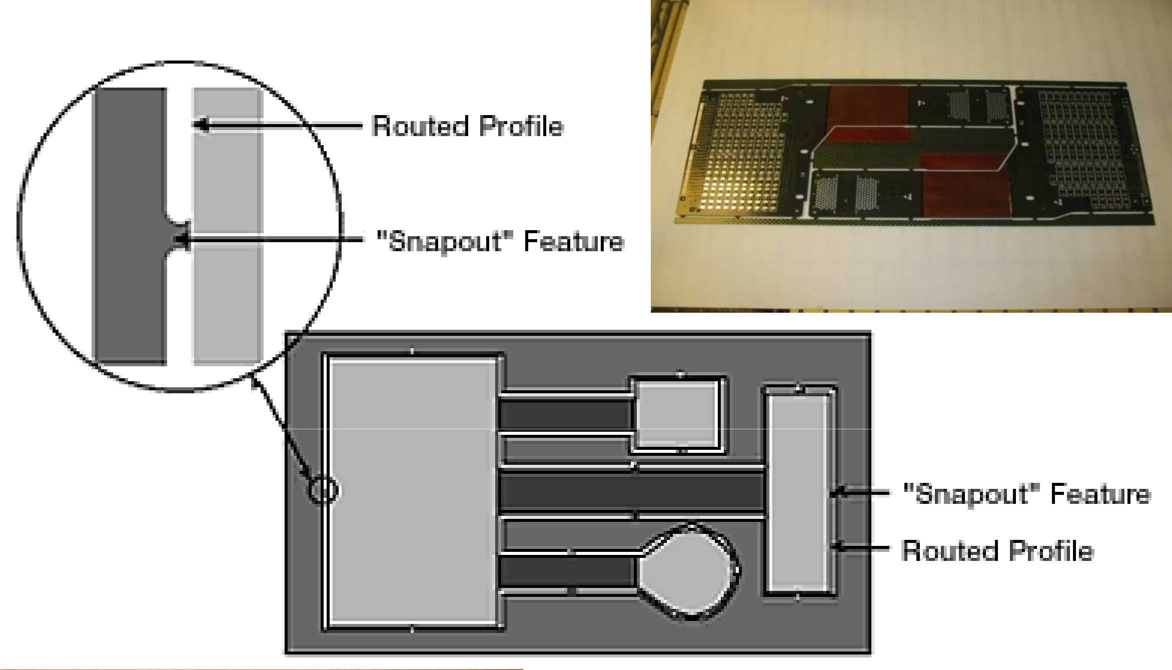
#	Impedance Type Name	Picture	Aff Layer	Line Width	Design Width	Cntr to Cntr	Ref Planes	tpd ps Atten dB	Rdc Rac ohms	L pH G umhos C pF	Pin-Pin pF	Sim ohms	Targ ohms	Predict ohms
1	Surface MS		L-1 None	10	5		None L-2	152 0.18	0.035 0.797	7589 527 3.0		50.01	50 +/- 5.0	50.01
2	EC Microstrip		L-1 None	5 5	5 5	10	None L-2	153 0.22	0.073 1.409	9932 433 2.4		99.48	100 +/- 10.0	99.48
3	Surface MS		L-1 None	3.7	5		None L-2	149 0.23	0.101 1.902	11110 362 2.0		74.72	75 +/- 7.5	74.72
4	Stripline		L-3 None	5	5		L-2 L-5	176 0.26	0.126 1.475	8856 612 3.5	62.5	50.23	50 +/- 5.0	50.23
5	Stripline		L-4 None	5	5		L-2 L-5	176 0.26	0.126 1.475	8856 612 3.5	62.5	50.23	50 +/- 5.0	50.23
6	EC Stripline		L-3 None	4 4	5 5	11	L-2 L-5	177 0.27	0.162 1.790	9745 559 3.2	62.0	99.98	100 +/- 10.0	99.98
7	EC Stripline		L-4 None	4 4	5 5	11	L-2 L-5	177 0.27	0.162 1.790	9745 559 3.2	62.0	99.98	100 +/- 10.0	99.98

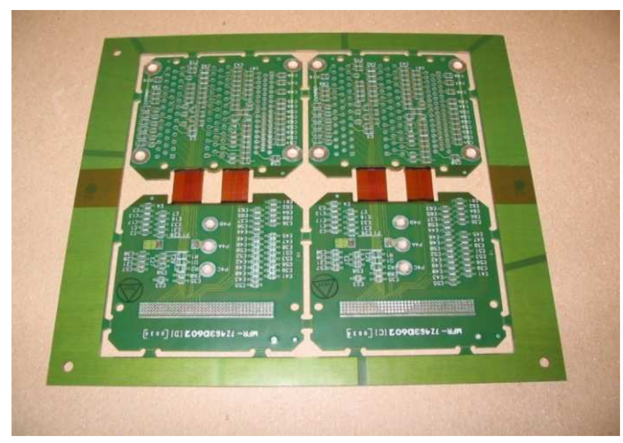


CAM

- CAD Data Analysis and Editing
- Production Panelization
- CNC Programming
- Electrical Test (ET) Programming

Assembly Sub-Panel ("Array")





PANEL UTILIZATION

Keep-out Area Perimeter

0.200”

1.0”

Impedance coupon

Tooling holes

Process control coupon

PCB

PCB

PCB

PCB

0.200”

1.0”

Manufacturing Panel

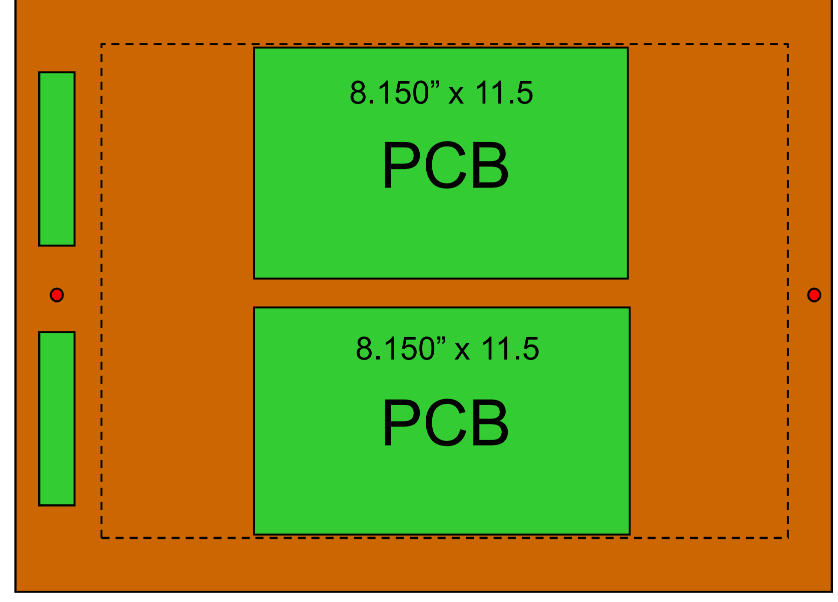
PANEL UTILIZATION

Very good panel utilization

8.150" x 11.150 PCB | 8.150" x 11.150 PCB
8.150" x 11.150 PCB | 8.150" x 11.150 PCB

Total usable area 371.25 in.^2 Total Circuit area 363.49 in.^2.
98% panel utilization

Poor panel utilization

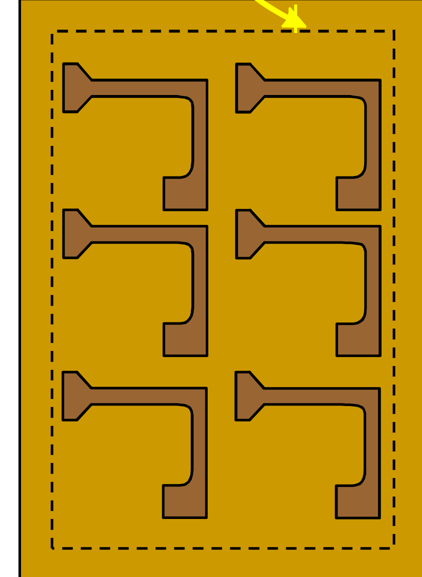


Total usable area 371.25 in.^2 Total Circuit area 187.45 in.^2.
50% panel utilization

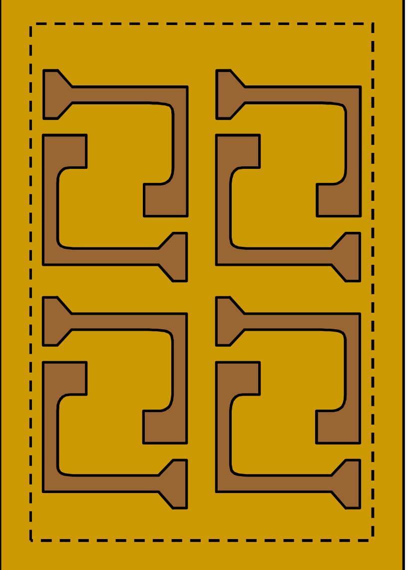
PANEL UTILIZATION: “Nesting”

Production Panel Size

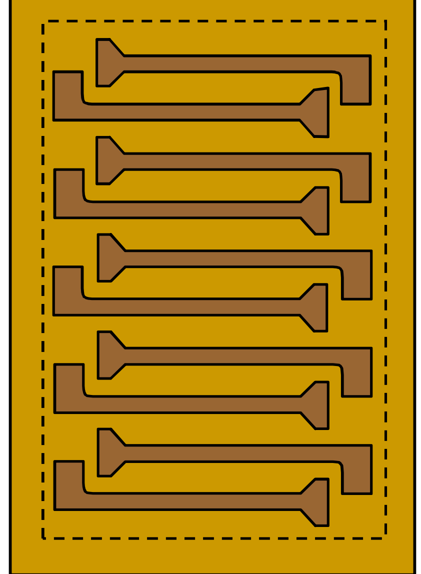
Usable Area



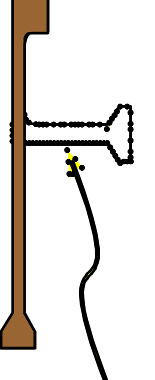
No Nesting
Panel Yield = 6 parts



Circuits Nested
Panel Yield = 8 parts



Optimized Nesting
Panel Yield =10 parts



Part folded to shape after punching

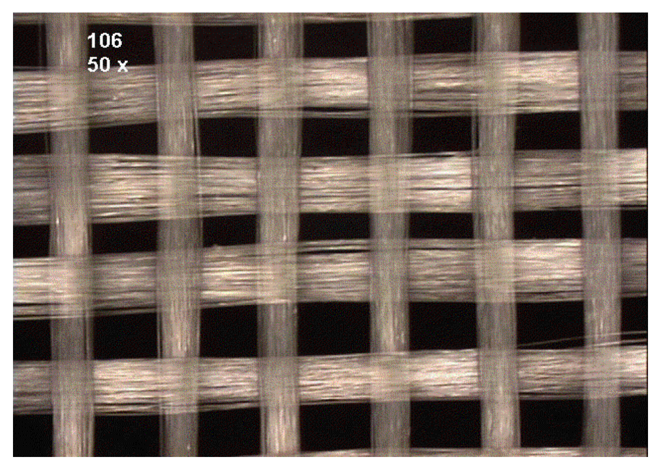
PCB Materials

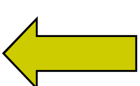
Core: PCB Building Block

Copper Foil: Typical Thickness
1/2oz (0.6 mils) or 1oz (1.2 mils)

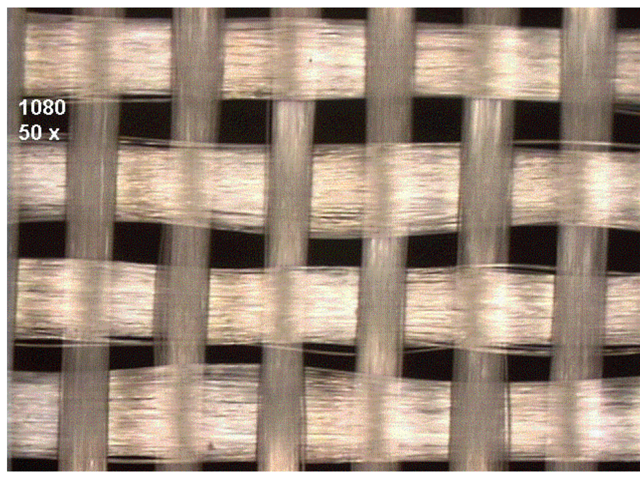
Dielectric: Thickness Ranges
.002”-.060” or greater
Glass Bundles & Organic Resin (“**FR4”**)
or high-performance specialty material
(Teflon, Ceramic, Polyimide, Low-Df, etc.)

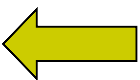
FR4 Woven Glass Styles





<u>Glass Style: 106</u>
Plain Weave
Count: 56x56 (ends/in)
Thickness: 0.0015”

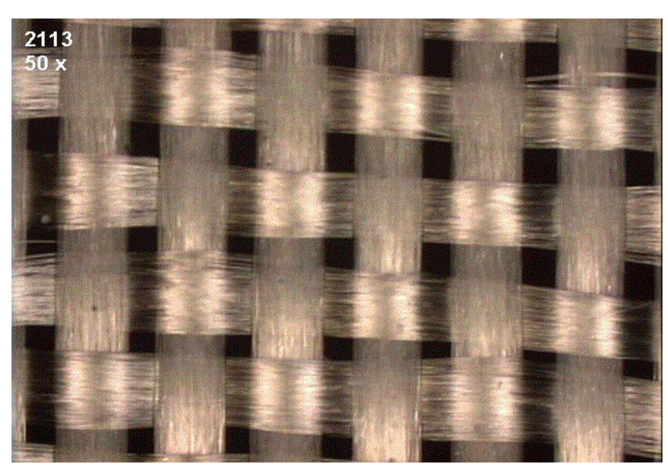


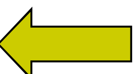


<u>Glass Style: 1080</u>
Plain Weave
Count: 60x47 (ends/in)
Thickness: 0.0025”

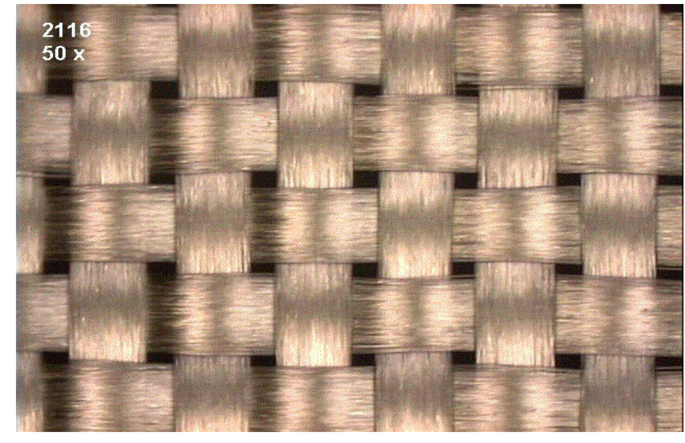
Source: Isola

FR4 Woven Glass Styles





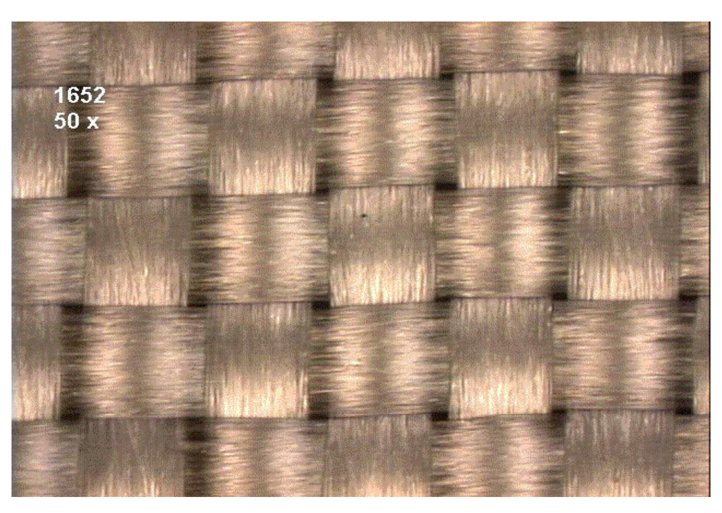
Glass Style: 2113
Plain Weave
Count: 60x56 (ends/in)
Thickness: 0.0029”

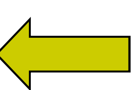


Glass Style: 2116
Plain Weave
Count: 60x58 (ends/in)
Thickness: 0.0038”

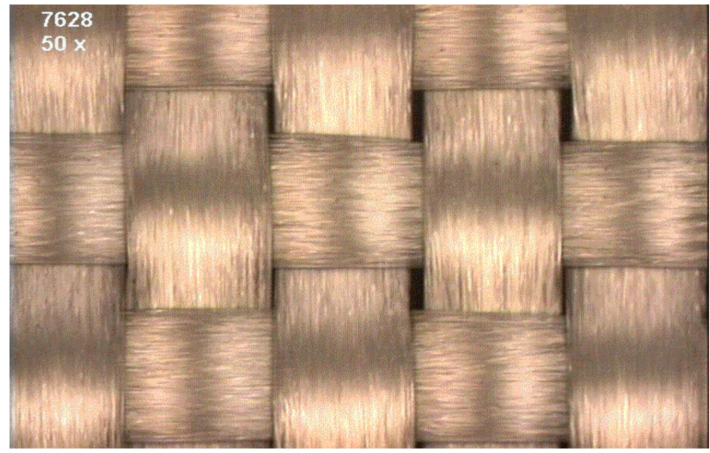
Source: Isola

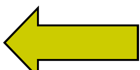
FR4 Woven Glass Styles





Glass Style: 1652
Plain Weave
Count: 52x52 (ends/in)
Thickness: 0.004”

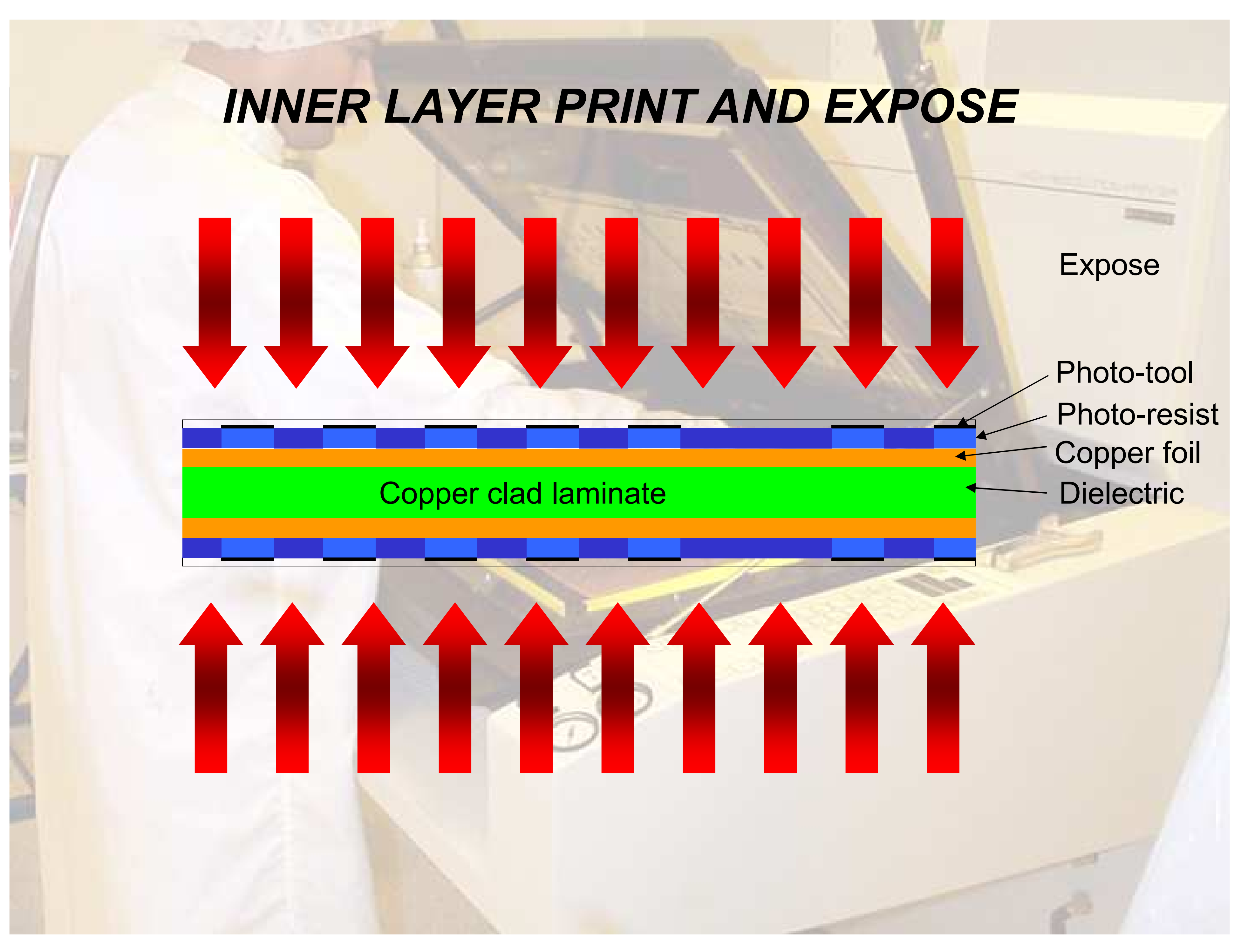




Glass Style: 7628
Plain Weave
Count: 44x32 (ends/in)
Thickness: 0.0068 (in)

Source: Isola

Production Processes

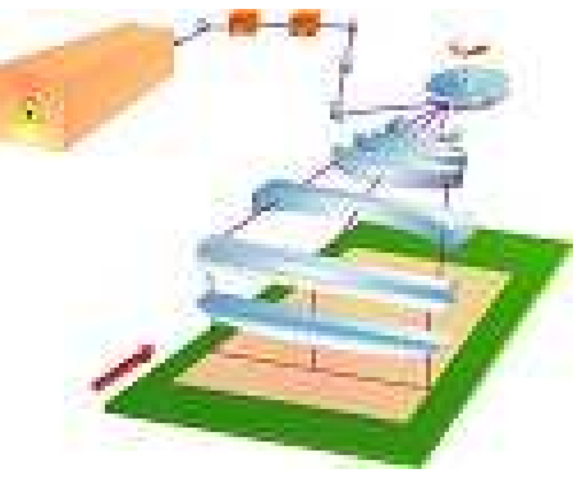

INNER LAYER PRINT AND EXPOSE
Expose
Photo-tool
Photo-resist
Copper foil
Dielectric
Copper clad laminate

Laser Direct Imaging (LDI)

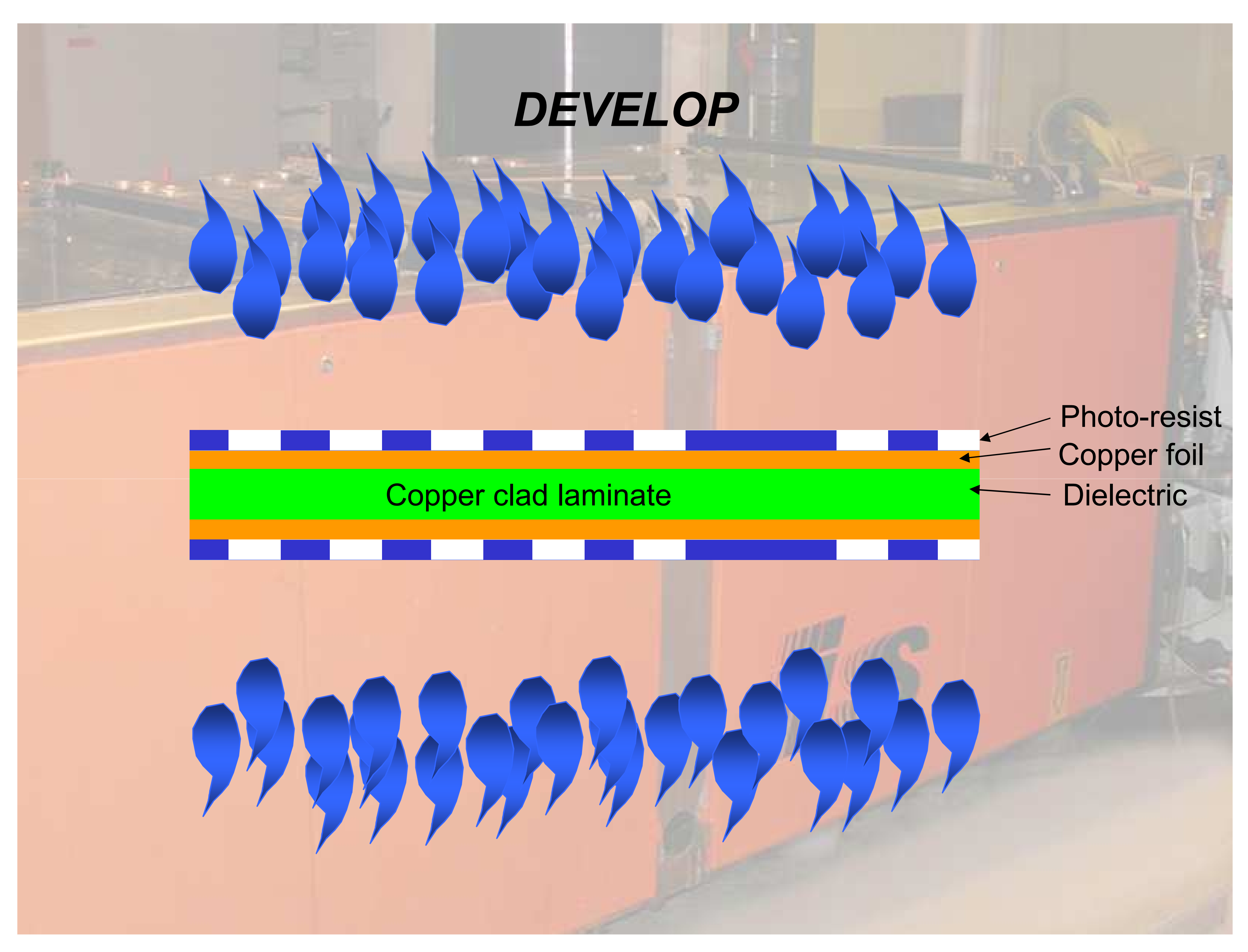
- Improved Resolution
- System Resolution 4000 dpi
- Current process capability (0.0025”/0.0025”)
- CCD Camera System & Target Fiducials
- Positional Accuracy +/-25µm (.001”)

Elimination of Photo Tools

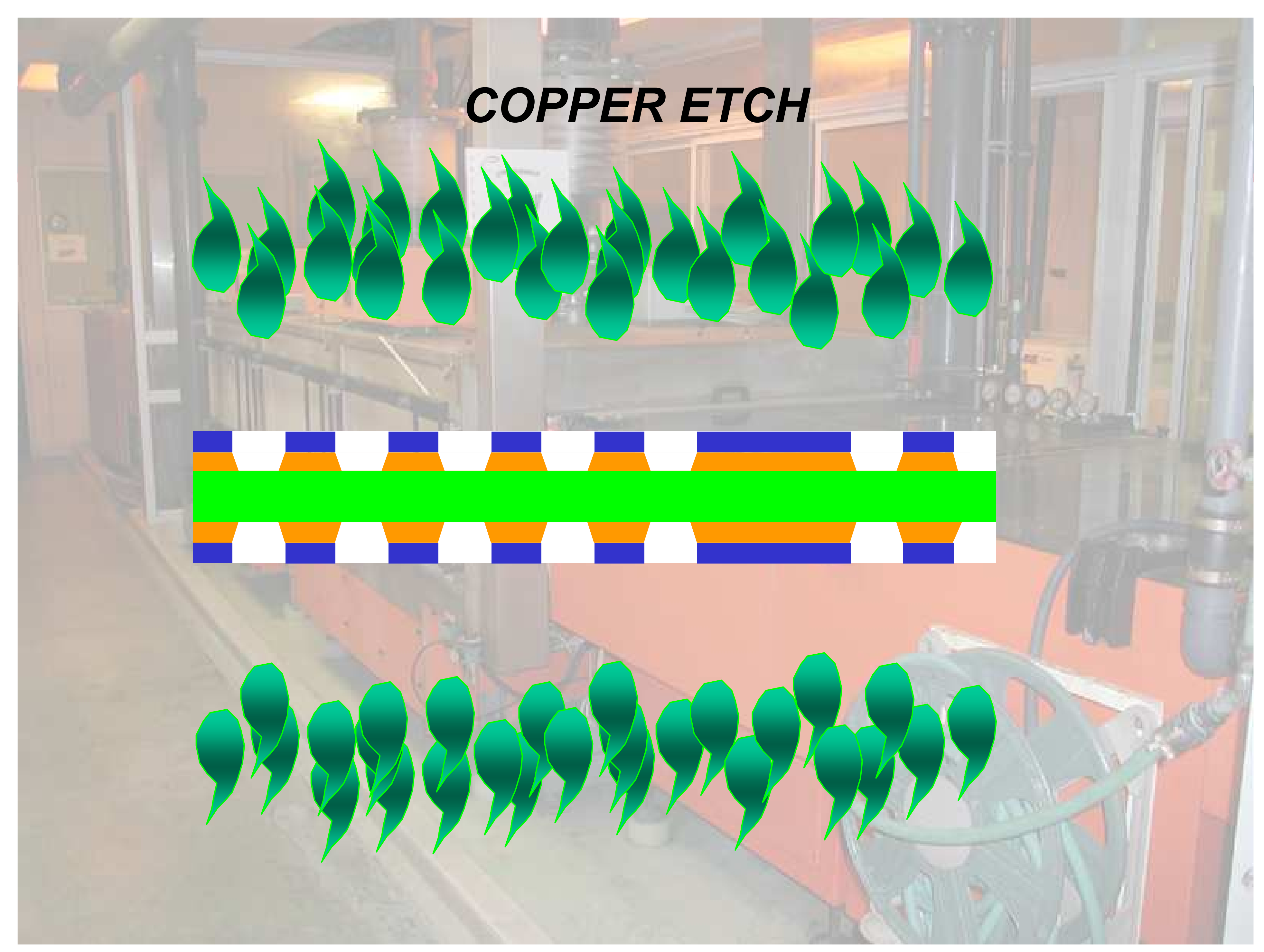
- No Film/Artwork Movement
- Quick Turn Made Easy
  - Run product as soon as Engineering releases data to the floor
- Reduction in Defect Count
  - Direct Write = No Film related defects
  - No issues related to loss of vacuum

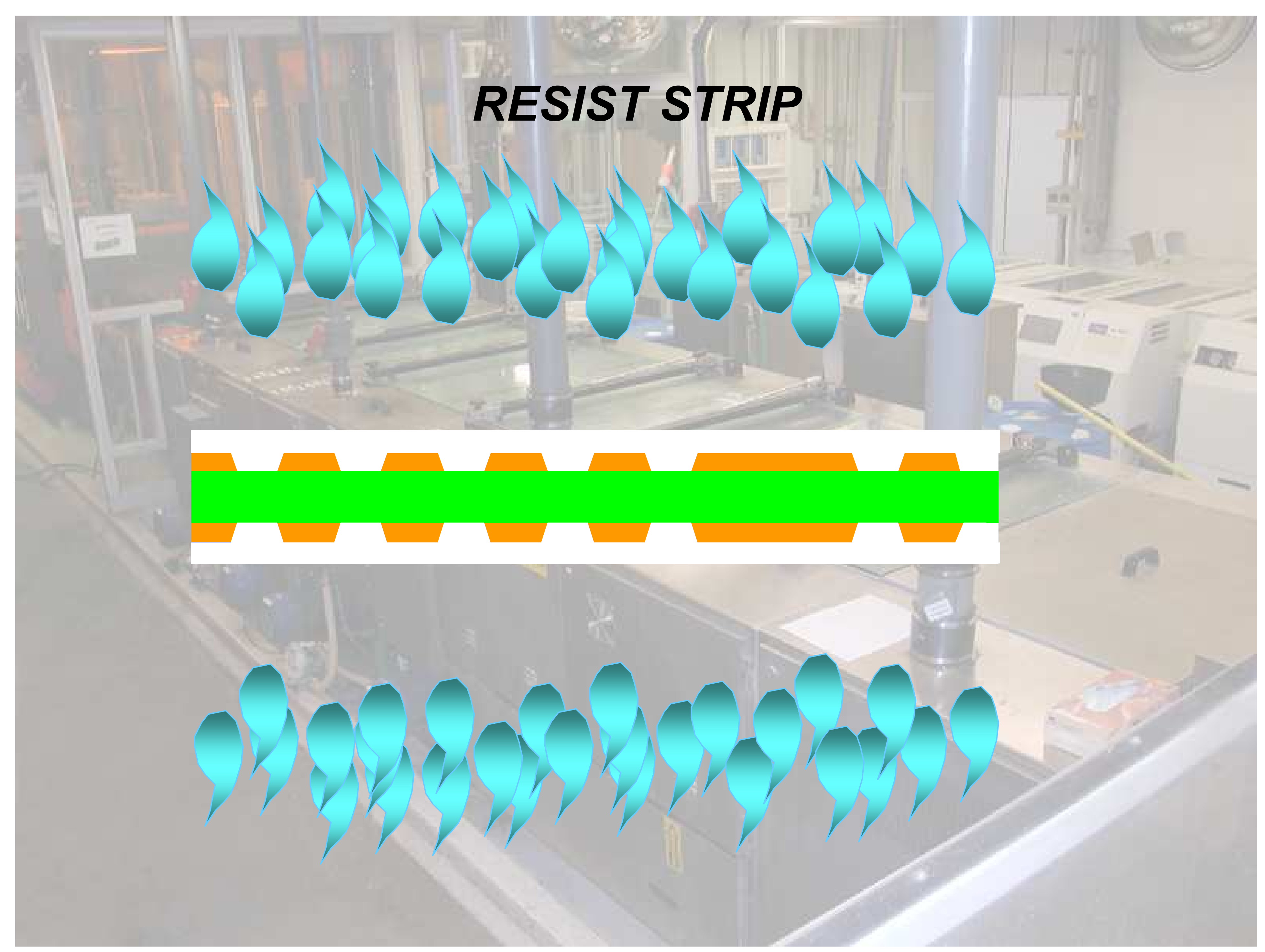


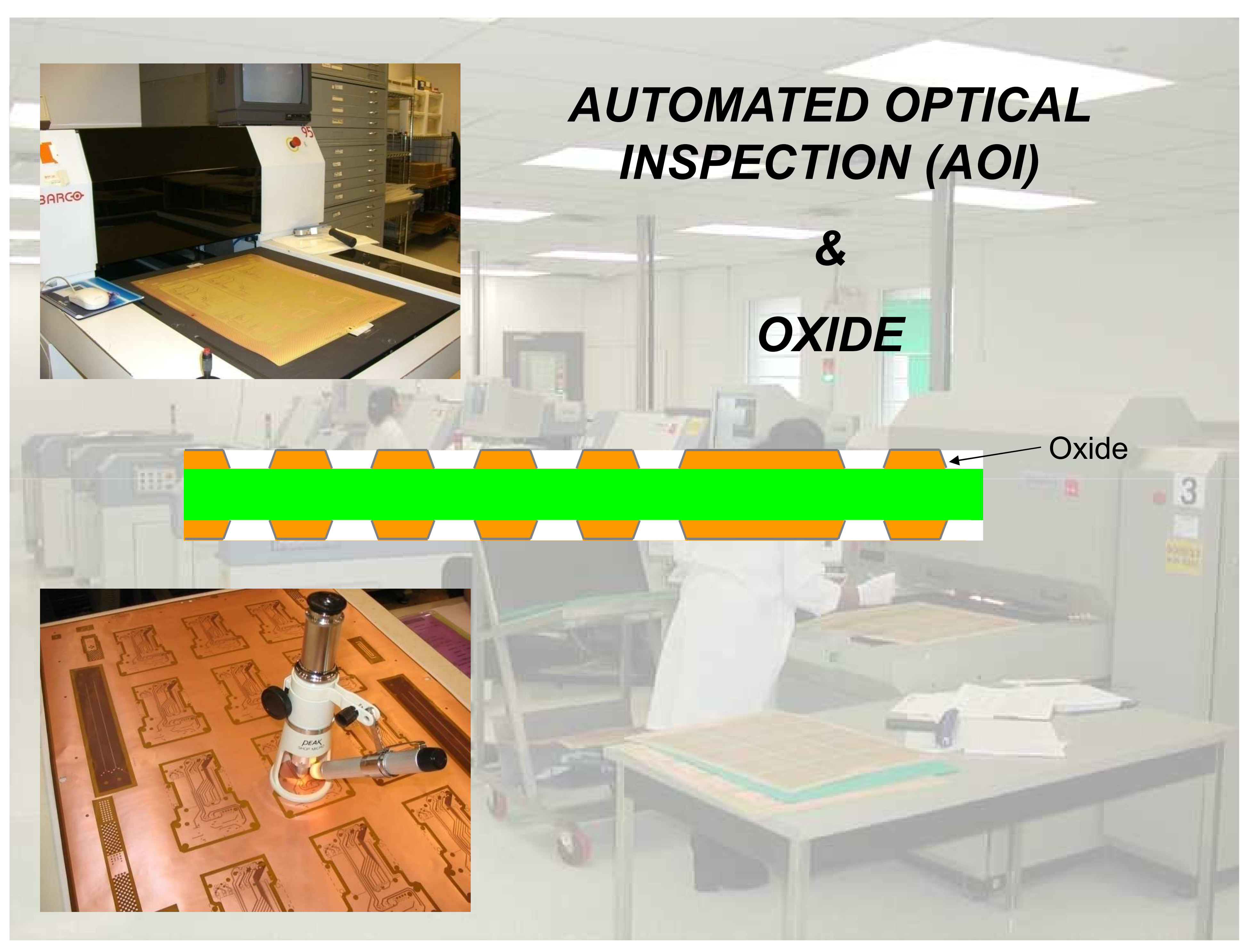
Scanning Optics

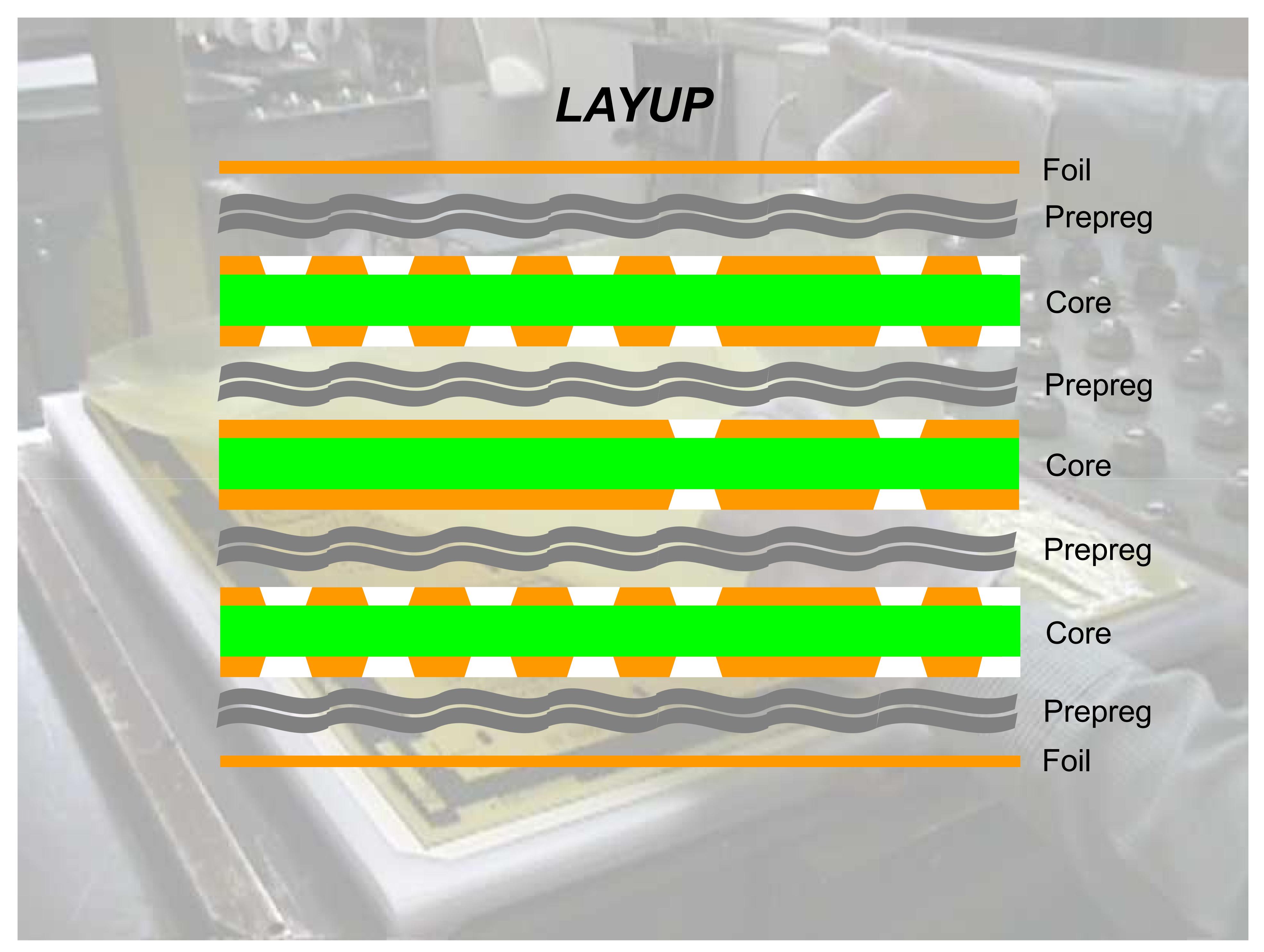


DEVELOP
Photo-resist
Copper foil
Dielectric
Copper clad laminate


COPPER ETCH


RESIST STRIP


AUTOMATED OPTICAL INSPECTION (AOI)
&
OXIDE
Oxide
BARCO

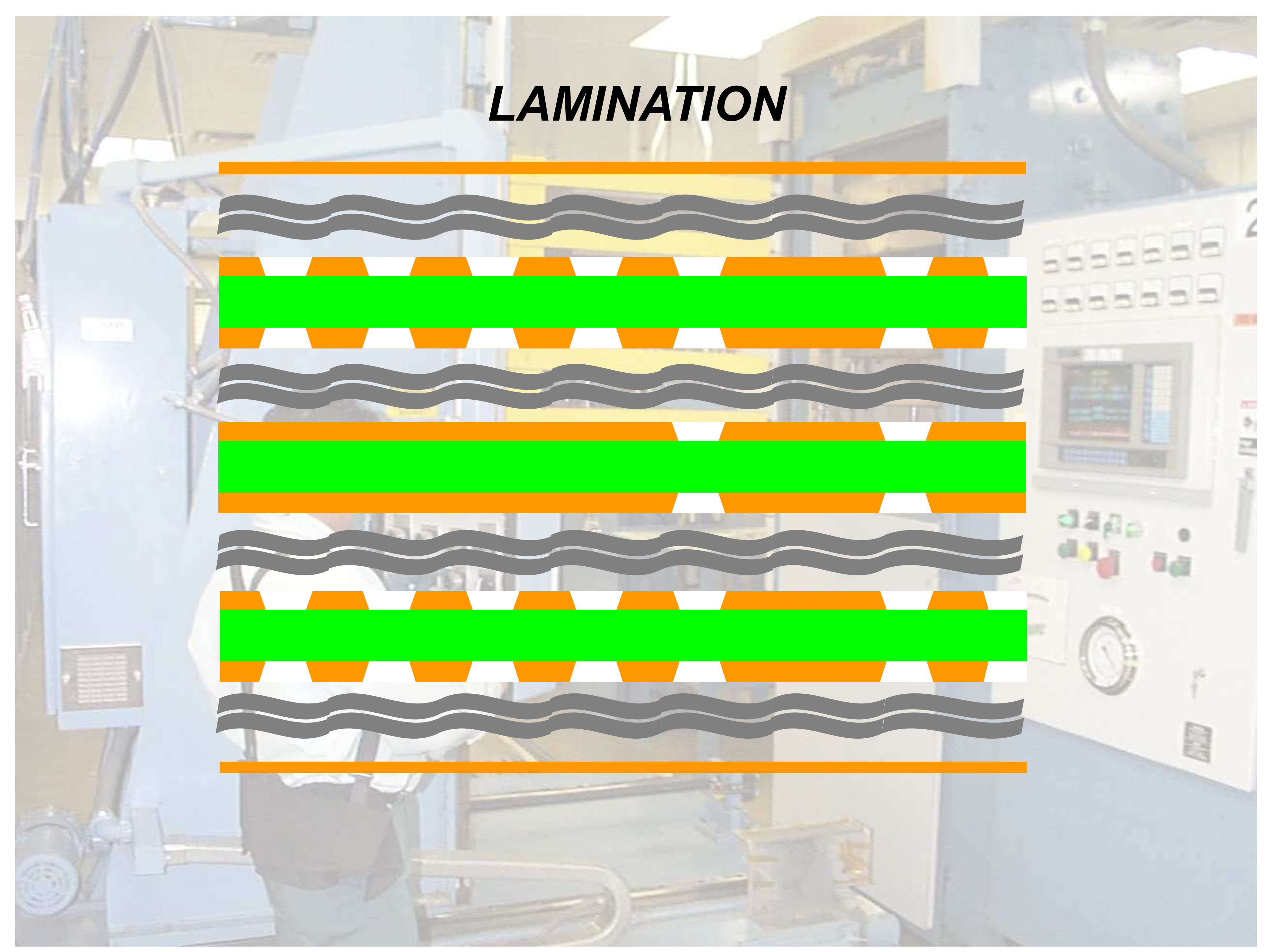

LAYUP
Foil
Prepreg
Core
Prepreg
Core
Prepreg
Core
Prepreg
Foil

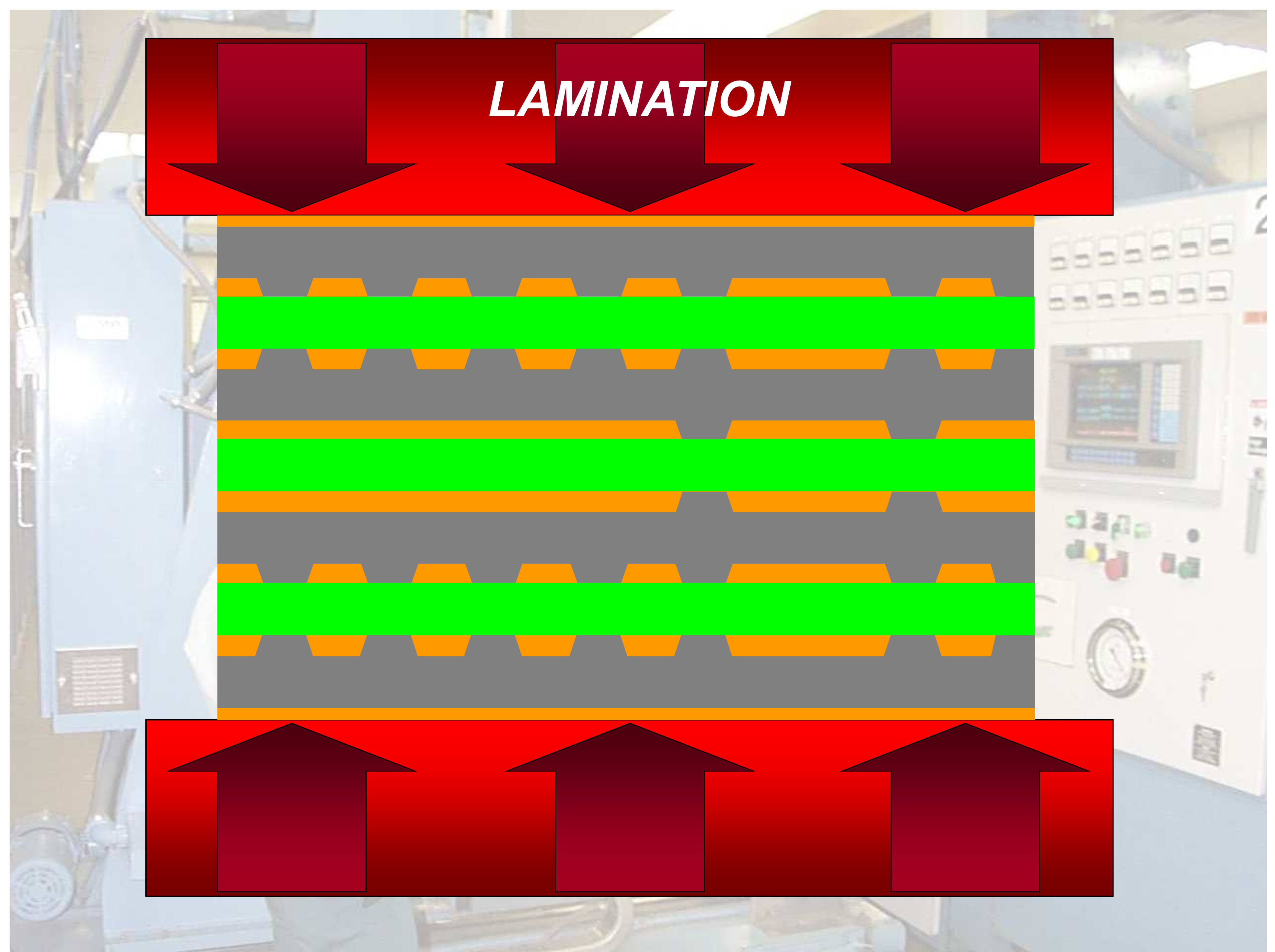
Stackup Example

Layer	Thickness	Rigid Stack	Description
	0.0005		Taiyo 4000-MP
Layer - 1	0.0020		**1/2oz Sig (Std Plt)**
	0.0043	106 106	370H
Layer - 2	0.0012		**1oz P/G**
	0.0060	0.0060 (1-1652)	370H
Layer - 3	0.0006		**1/2oz Sig**
	0.0090	1080 1080 1080	370H
Layer - 4	0.0012		**1oz P/G**
	0.0142	0.0140 (2-7628)	370H
Layer - 5	0.0012		**1oz P/G**
	0.0090	1080 1080 1080	370H
Layer - 6	0.0006		**1/2oz Sig**
	0.0060	0.0060 (1-1652)	370H
Layer - 7	0.0012		**1oz P/G**
	0.0043	106 106	370H
Layer - 8	0.0020		**1/2oz Sig (Std Plt)**
	0.0005		Taiyo 4000-MP

LAMINATION
tmp
CORETEC
STOP
MAIN DISCONNECT
DANGER
PINCH POINT
High Voltage
SOUTHWORTH

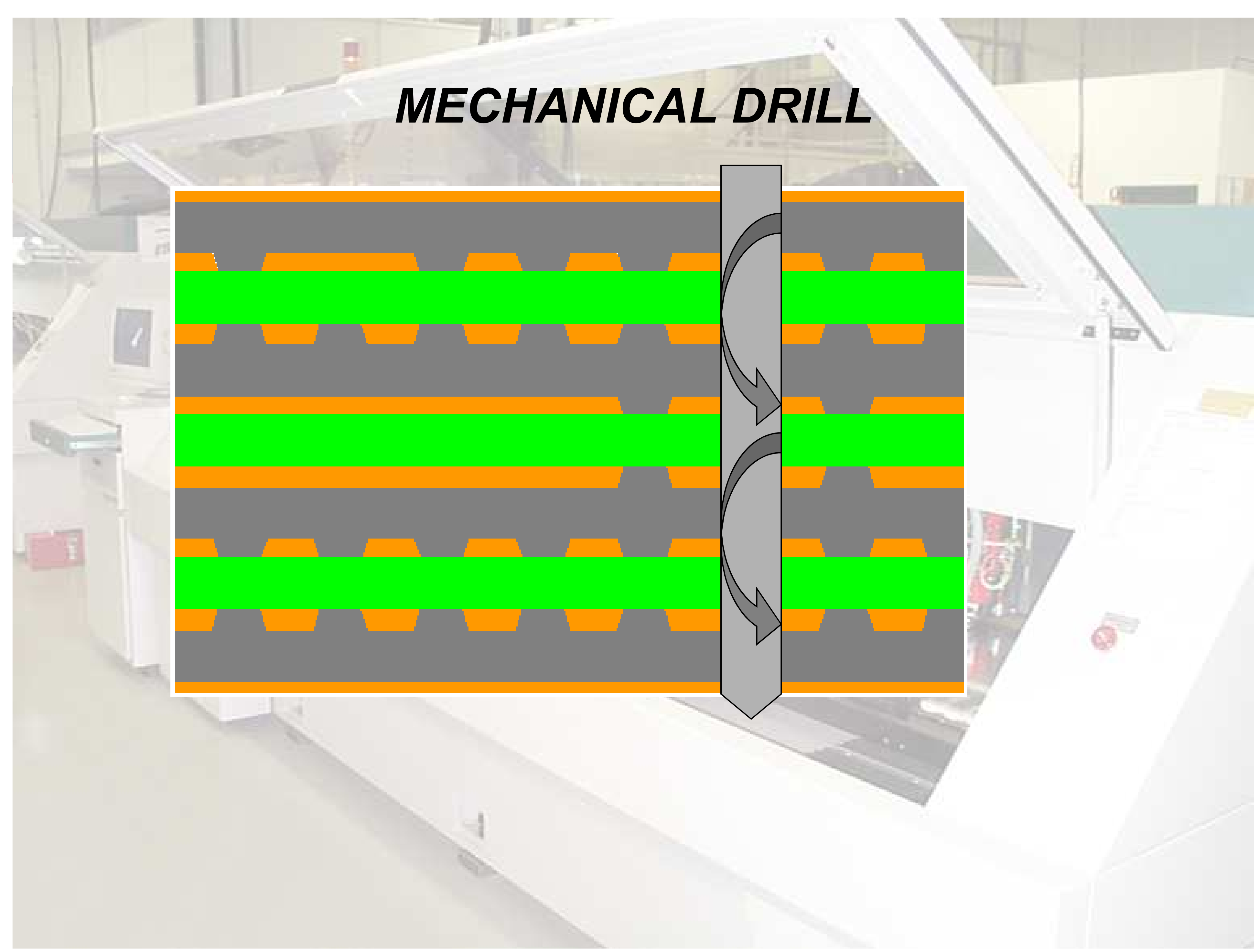
LAMINATION




LAMINATION

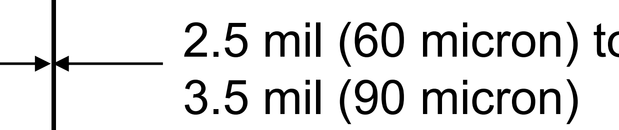
MECHANICAL DRILL
DO NOT RUN MACHINE
WITH HOOD OPEN
EXCELLON

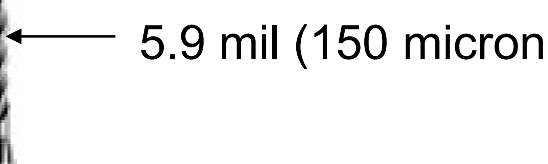
MECHANICAL DRILL



Small Diameter Mechanical Drills

Human hair



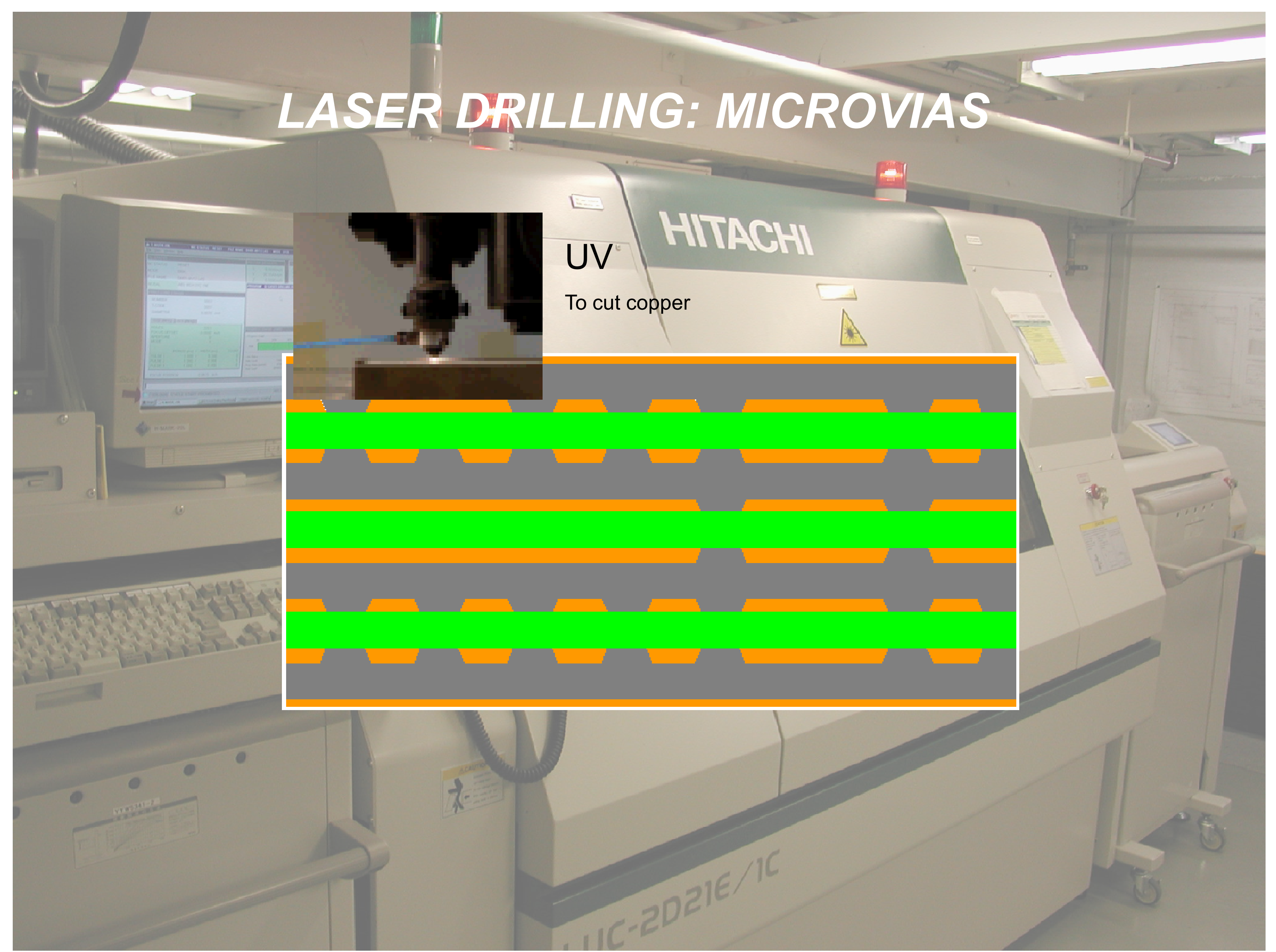


Carbide drill bit

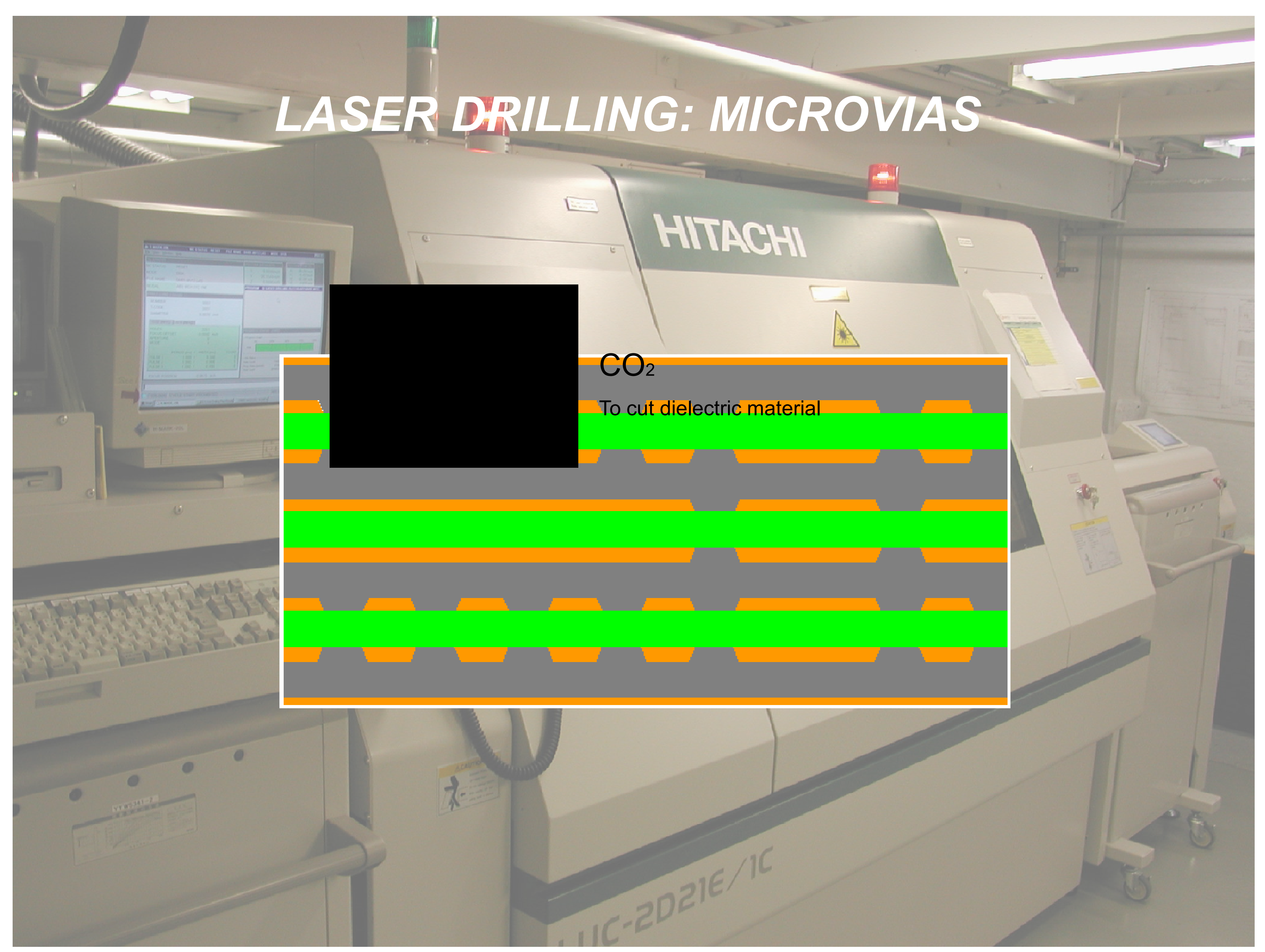
- Small diameter are very fragile
- High speed spindles are required
- Feed rates are about 50% of standard via diameters
- Drill life of 300 to 600 hits depending on material
- Short flute length limits hole depth
- Drill cost is higher

Via Structures: Thru-Hole, Blind, Buried

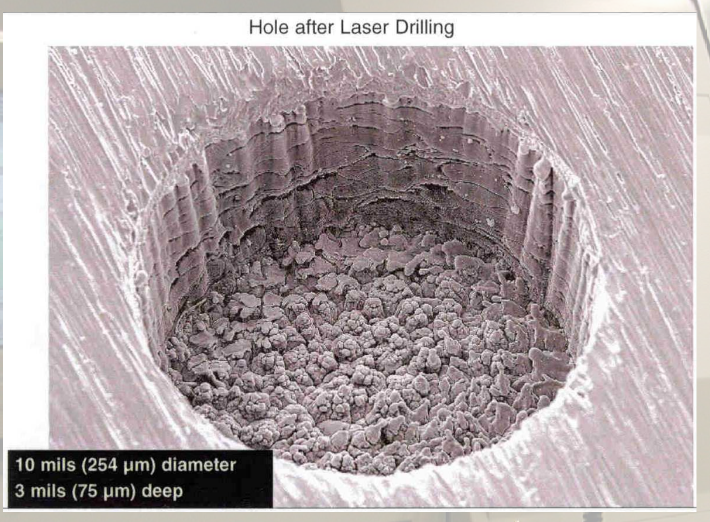
MICROVIAS: DRIVEN BY TIGHT SPACING

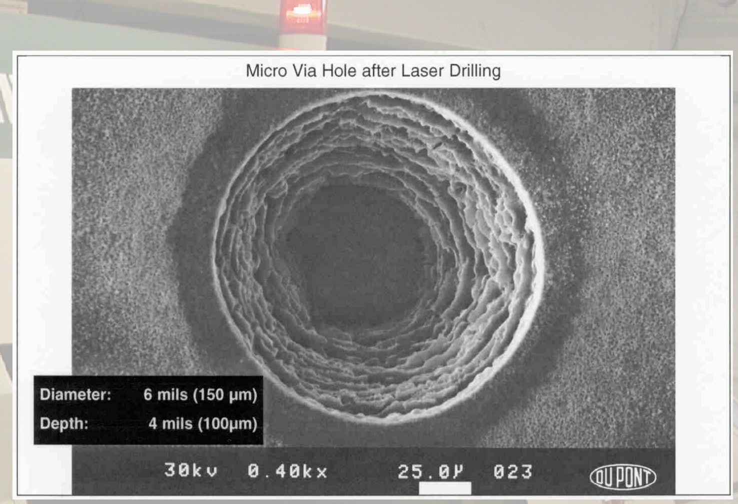

LASER DRILLING: MICROVIAS
UV
To cut copper
HITACHI

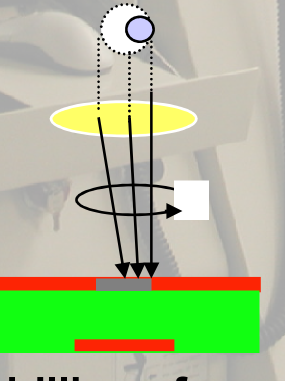
LASER DRILLING: MICROVIAS



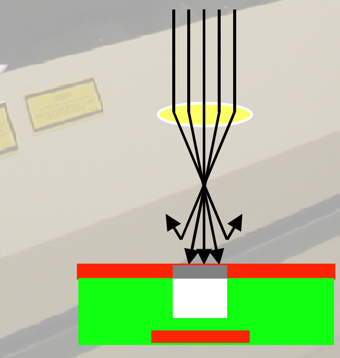
LASER DRILLING: MICROVIAS







U.V. drilling of copper using focused, spiraling beam



CO_2 drilling of laminate dielectric using refracted beam

DESMEAR: PLASMA OR CHEMICAL

HOLE PREPARATION

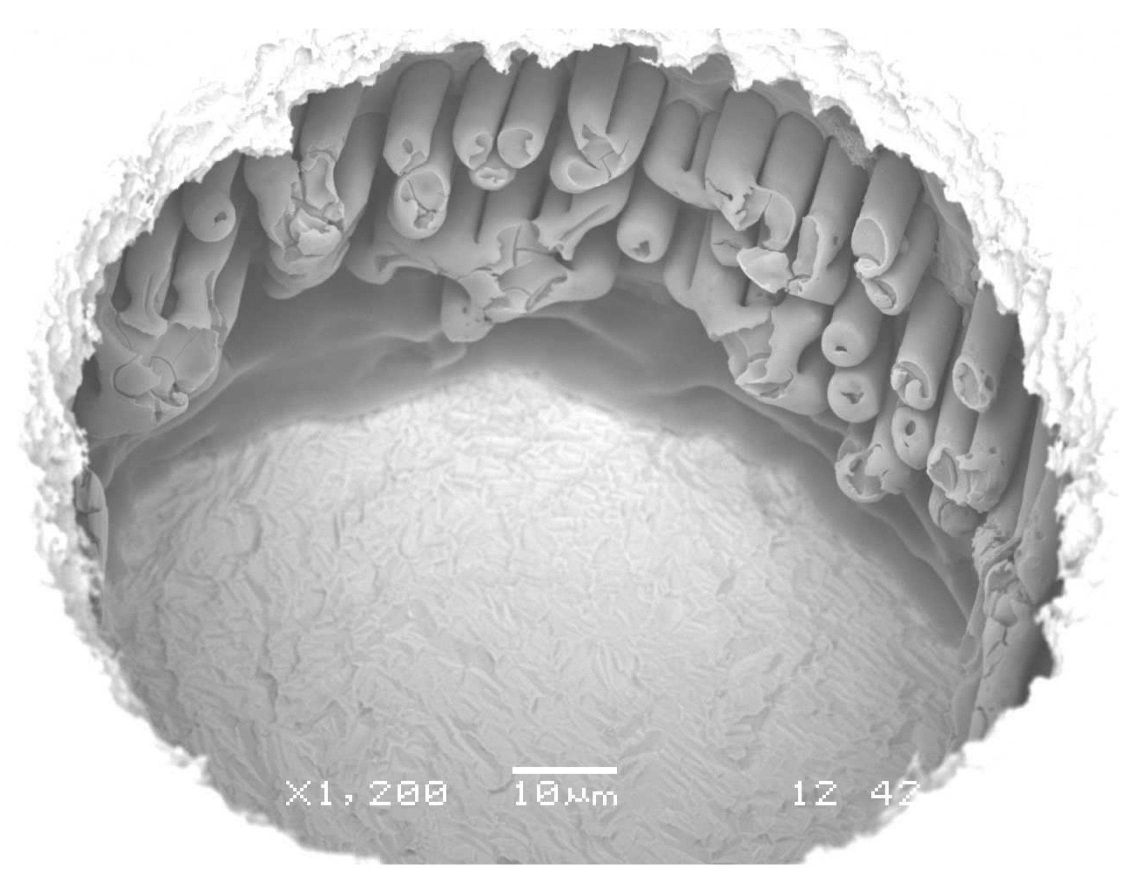
As Drilled

HOLE PREPARATION

504X 4KV WD:8MM S:00000 P:00004
100UM
CARLTON COMELIM 1 1.2MM

After Desmear

HOLE PREPARATION



Laser Microvia Post-Desmear

ETCHBACK

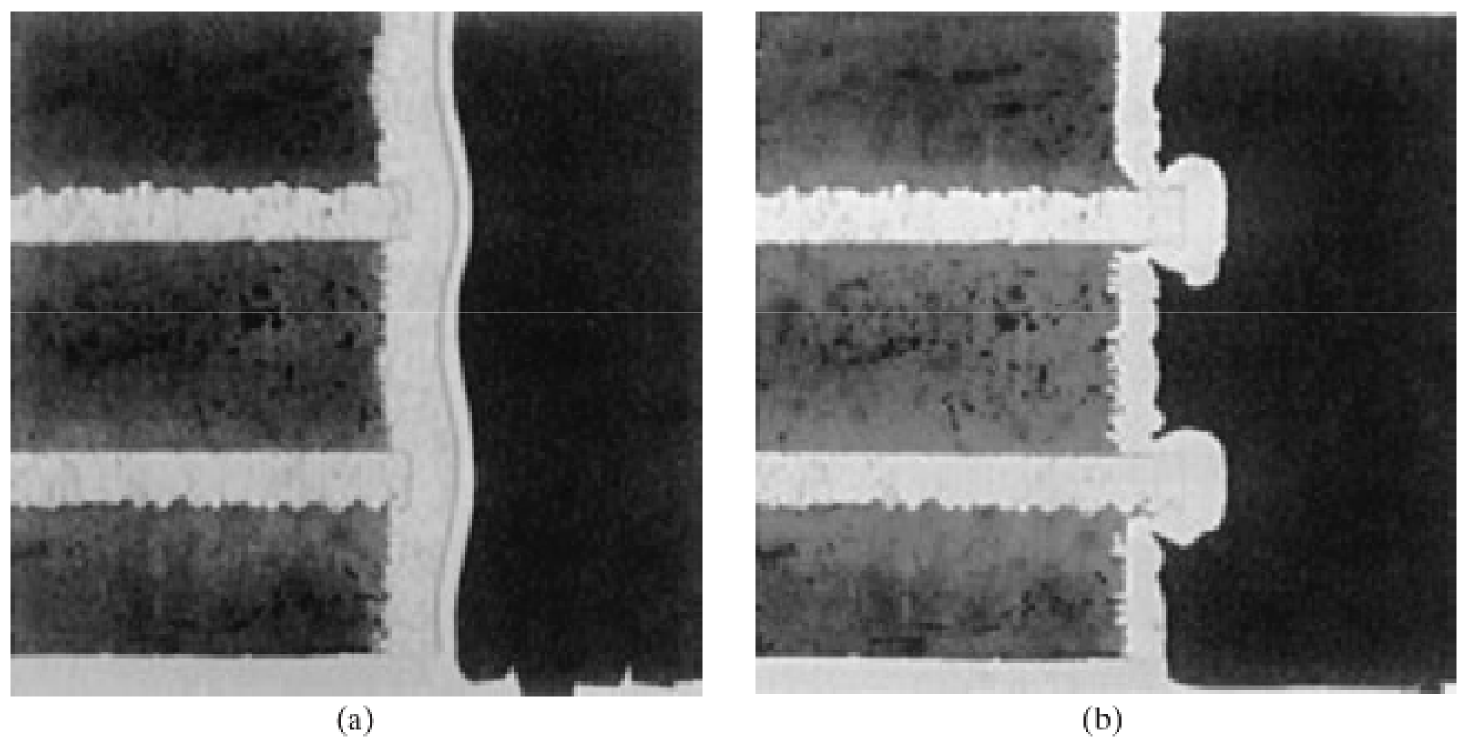
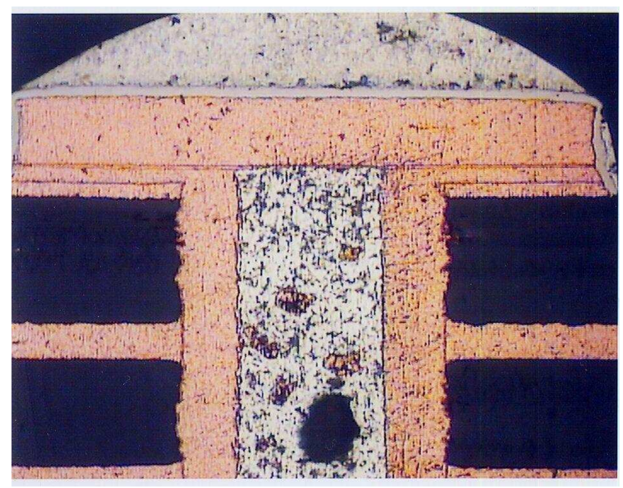
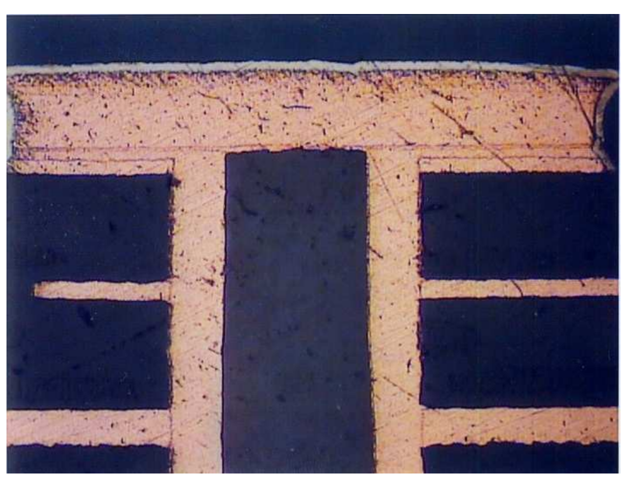


FIGURE 48.34 Etchback. (*a*) Target: uniform etchback of base laminate; uniform plating in the plated through-hole. (*b*) Nonconforming: nonuniform and excessive etchback of base laminate results in unacceptable nonuniform plating in the hole. *(Source: IPC.)*

Hole Fill: “Via-in-Pad”





Conductive Via fill

Non-conductive Via fill

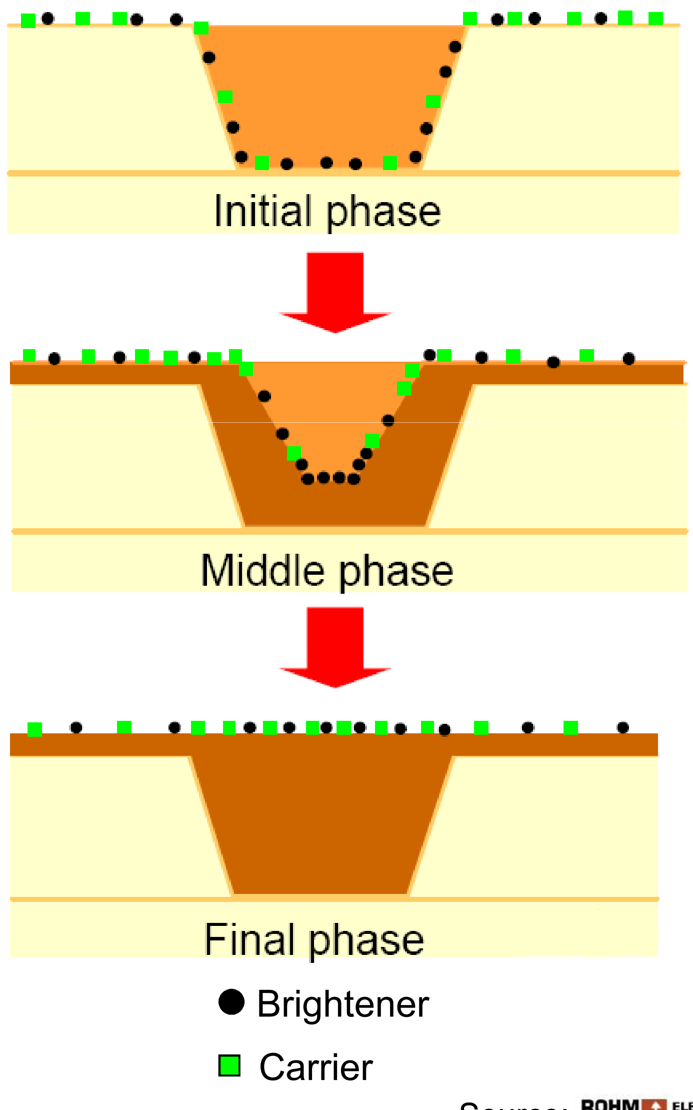
Via Hole Fill Equipment

Vacuum Assist Via Filling

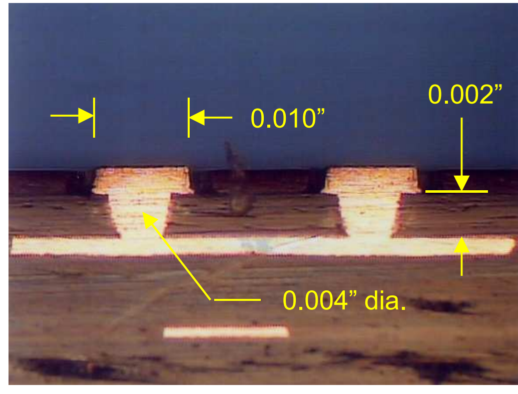
Automated Linear Surface Grinder

Excess (Cured) Fill Material Removed

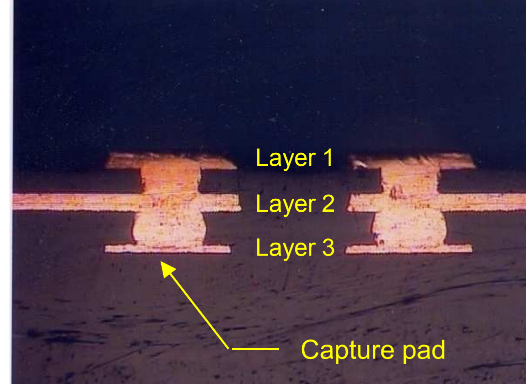
Microvia Copper Fill



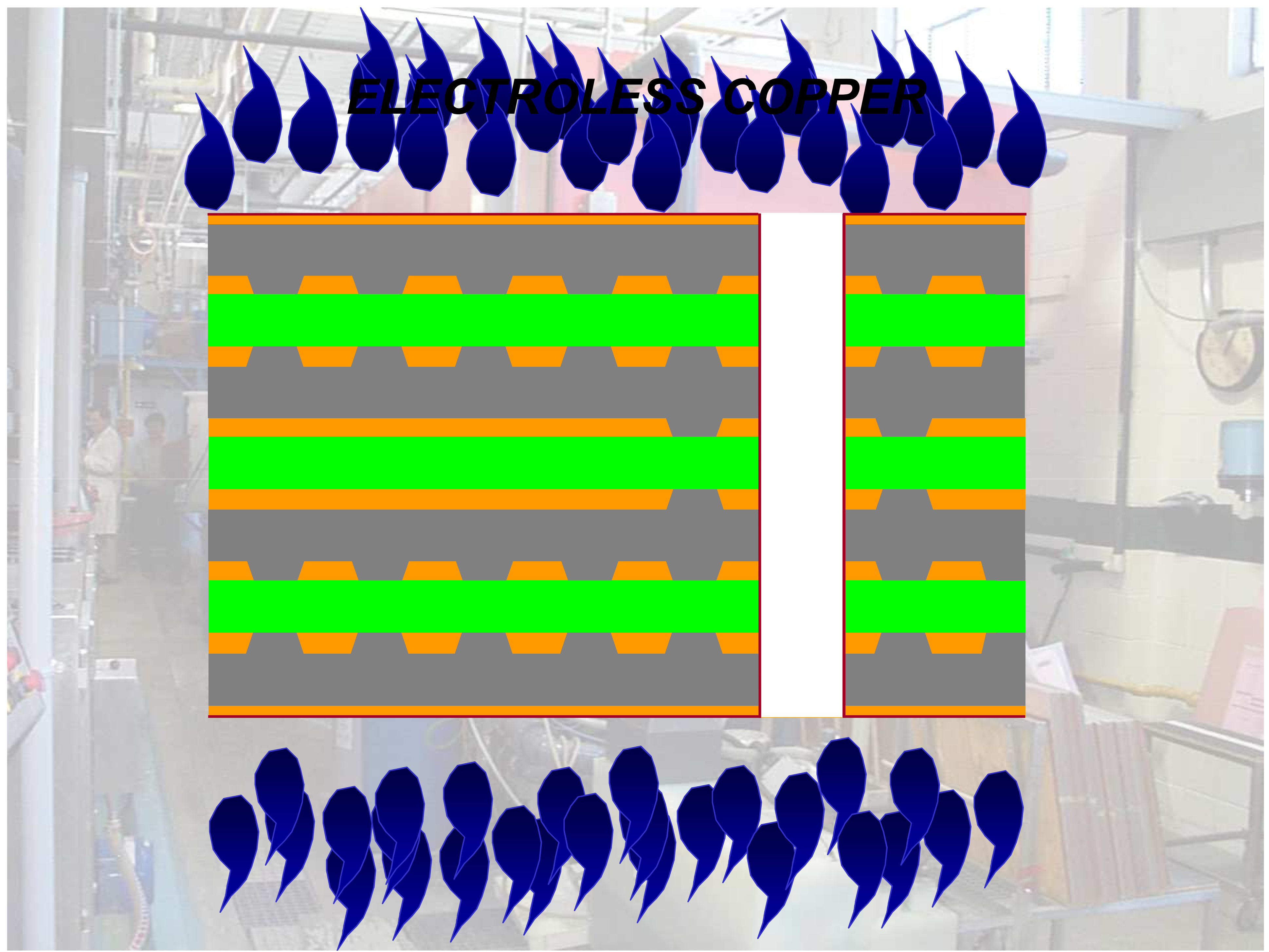
Planar Microvia

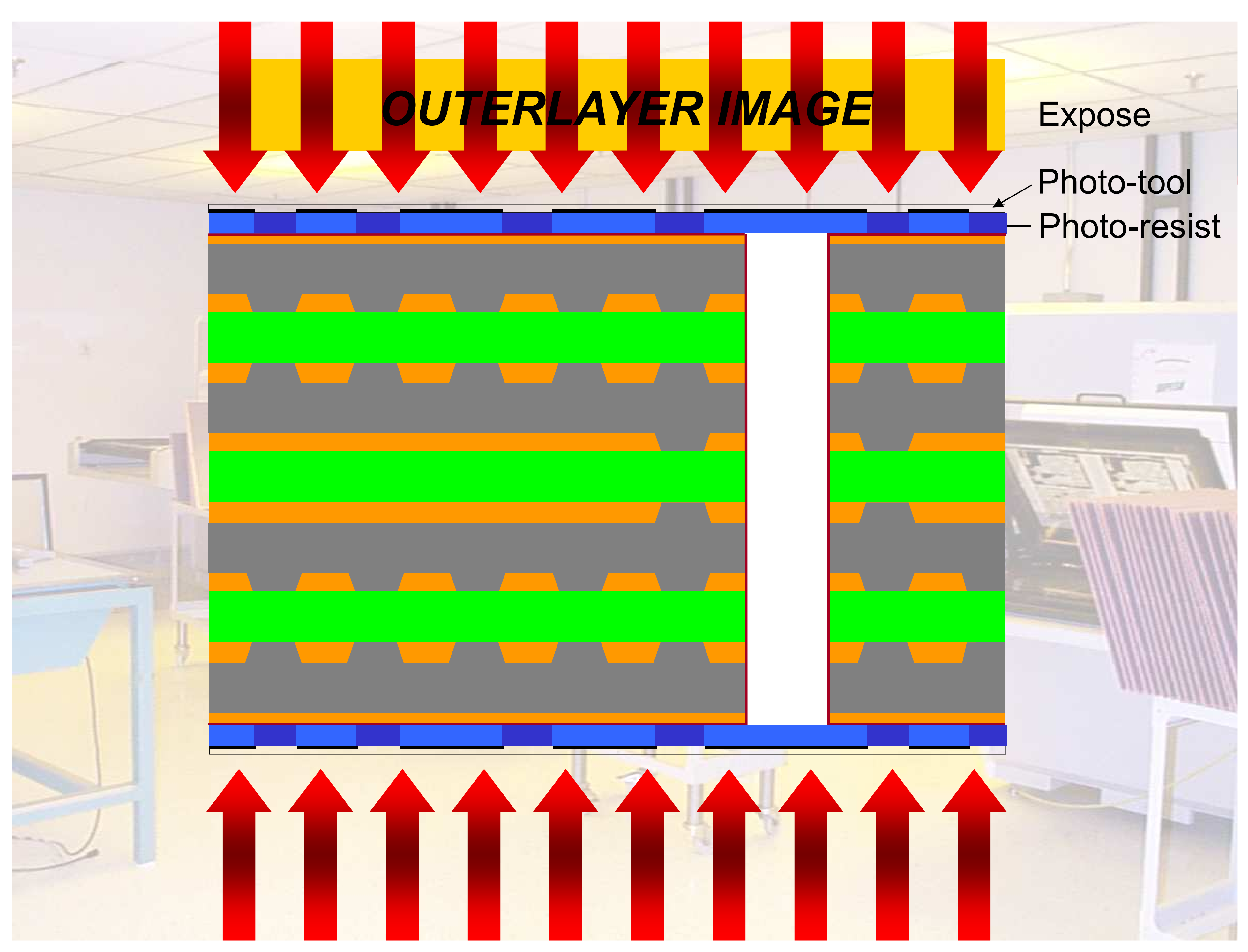


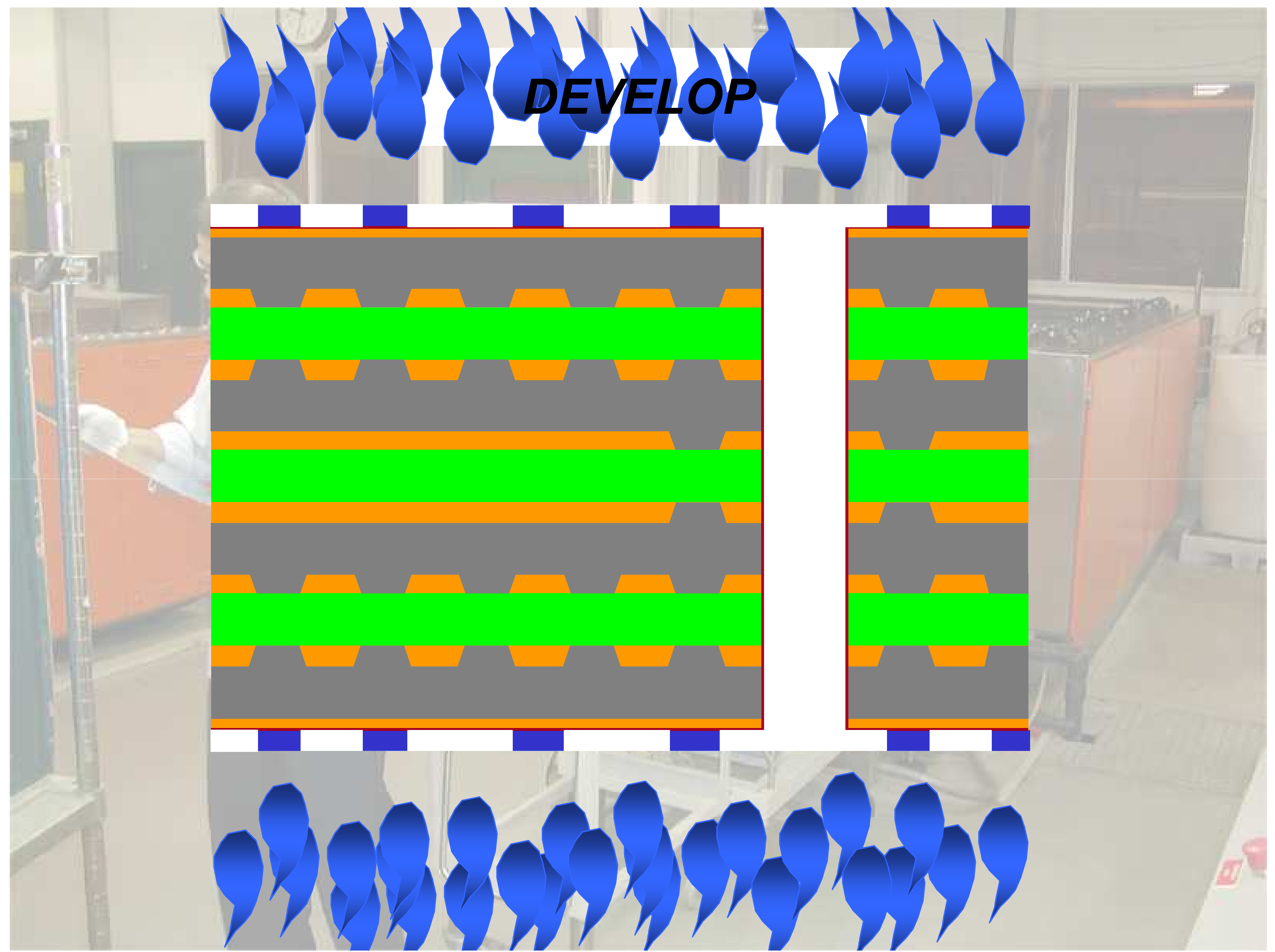
Stacked Microvia



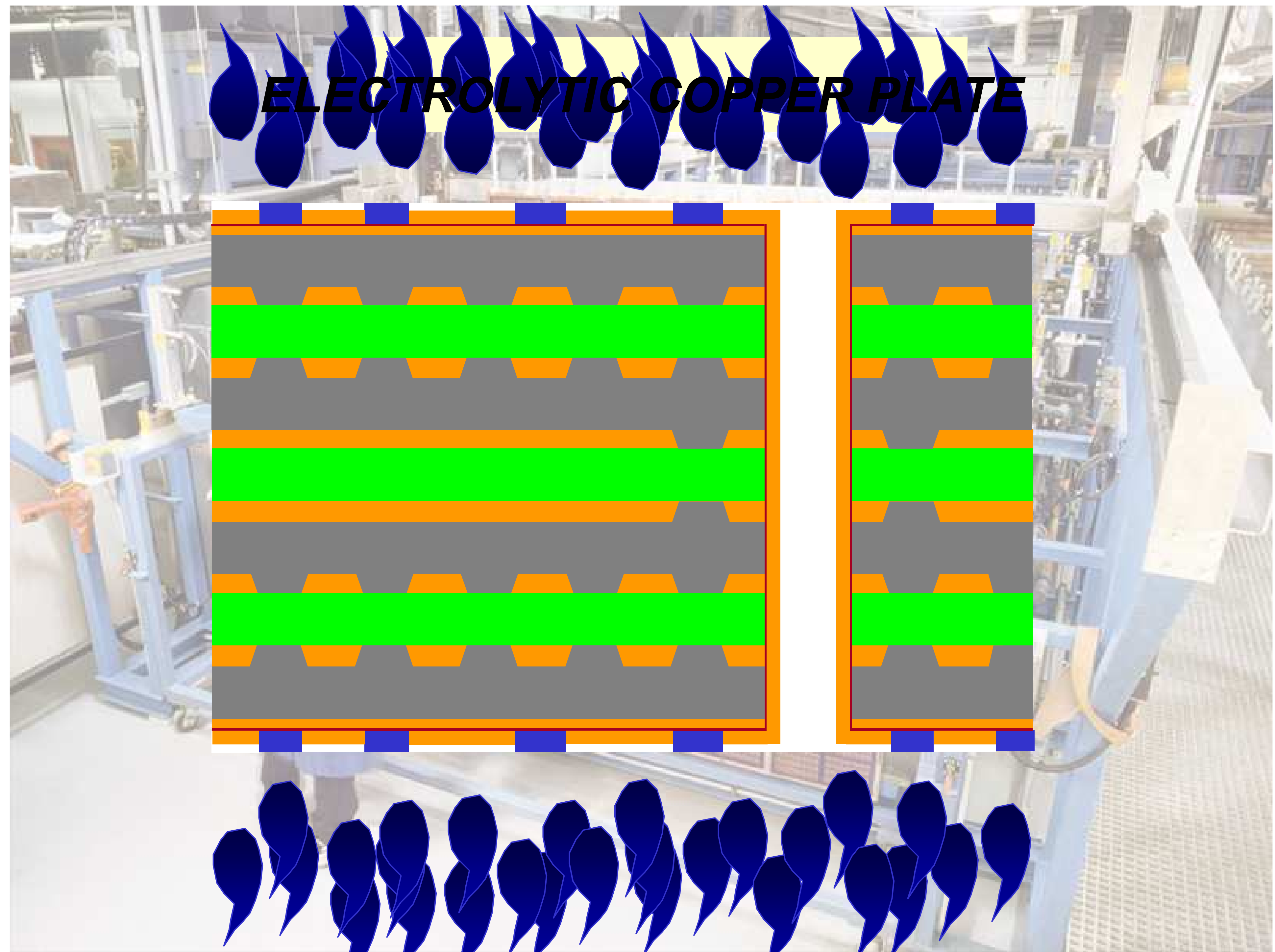
Source: ROHM AND HAAS ELECTRONIC MATERIALS CIRCUIT BOARD TECHNOLOGIES

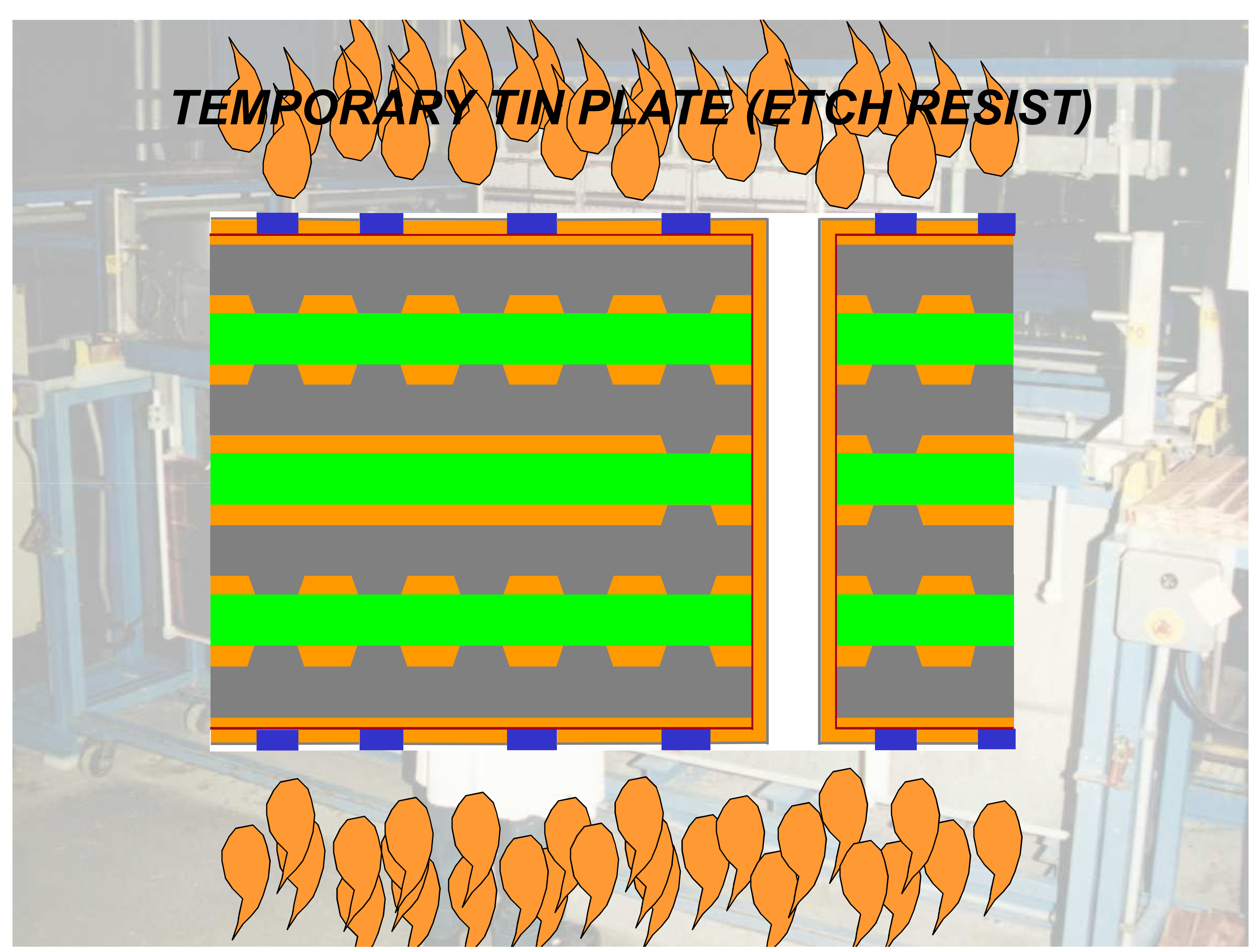

ELECTROLESS COPPER

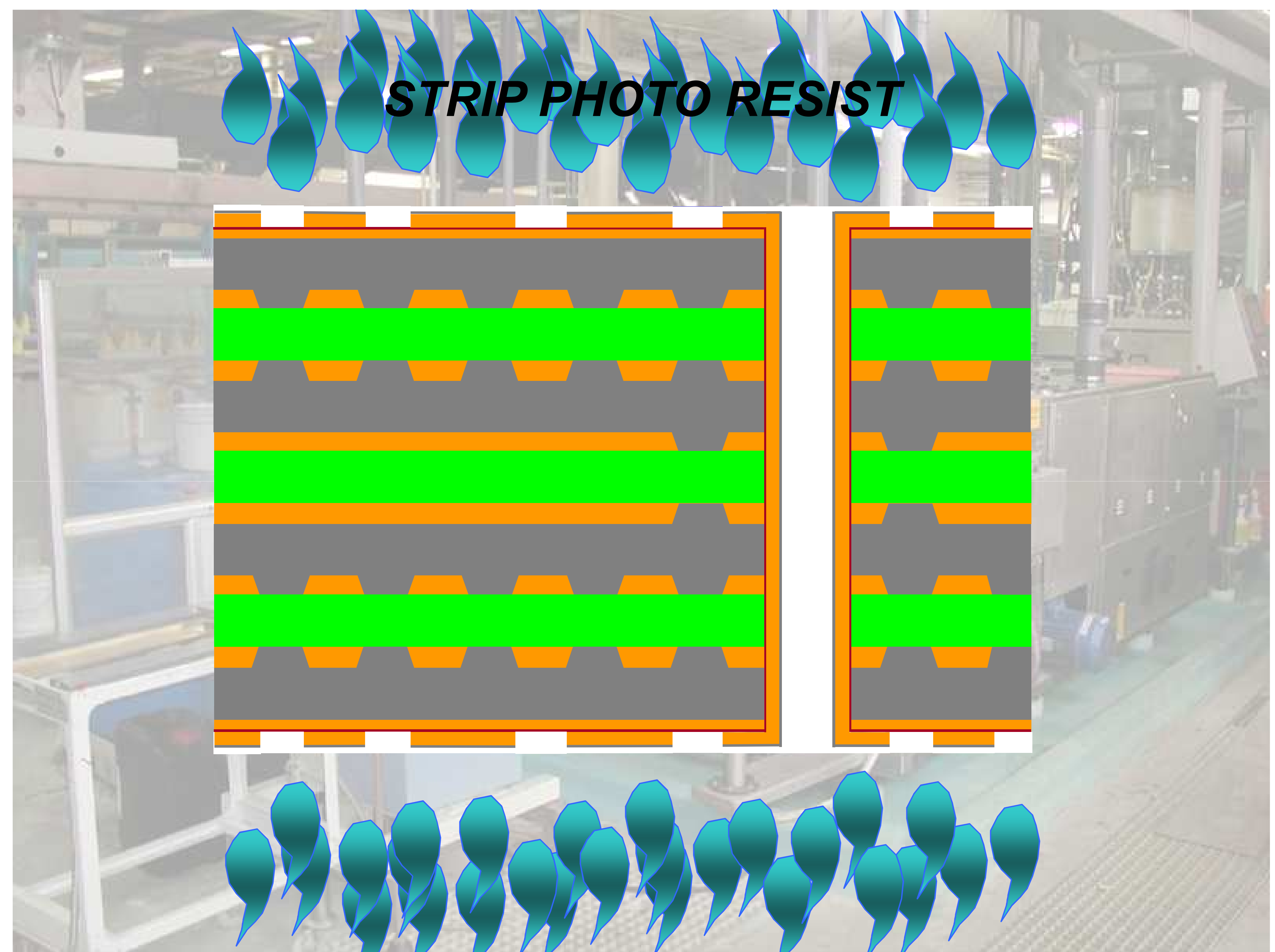

OUTERLAYER IMAGE
Expose
Photo-tool
Photo-resist

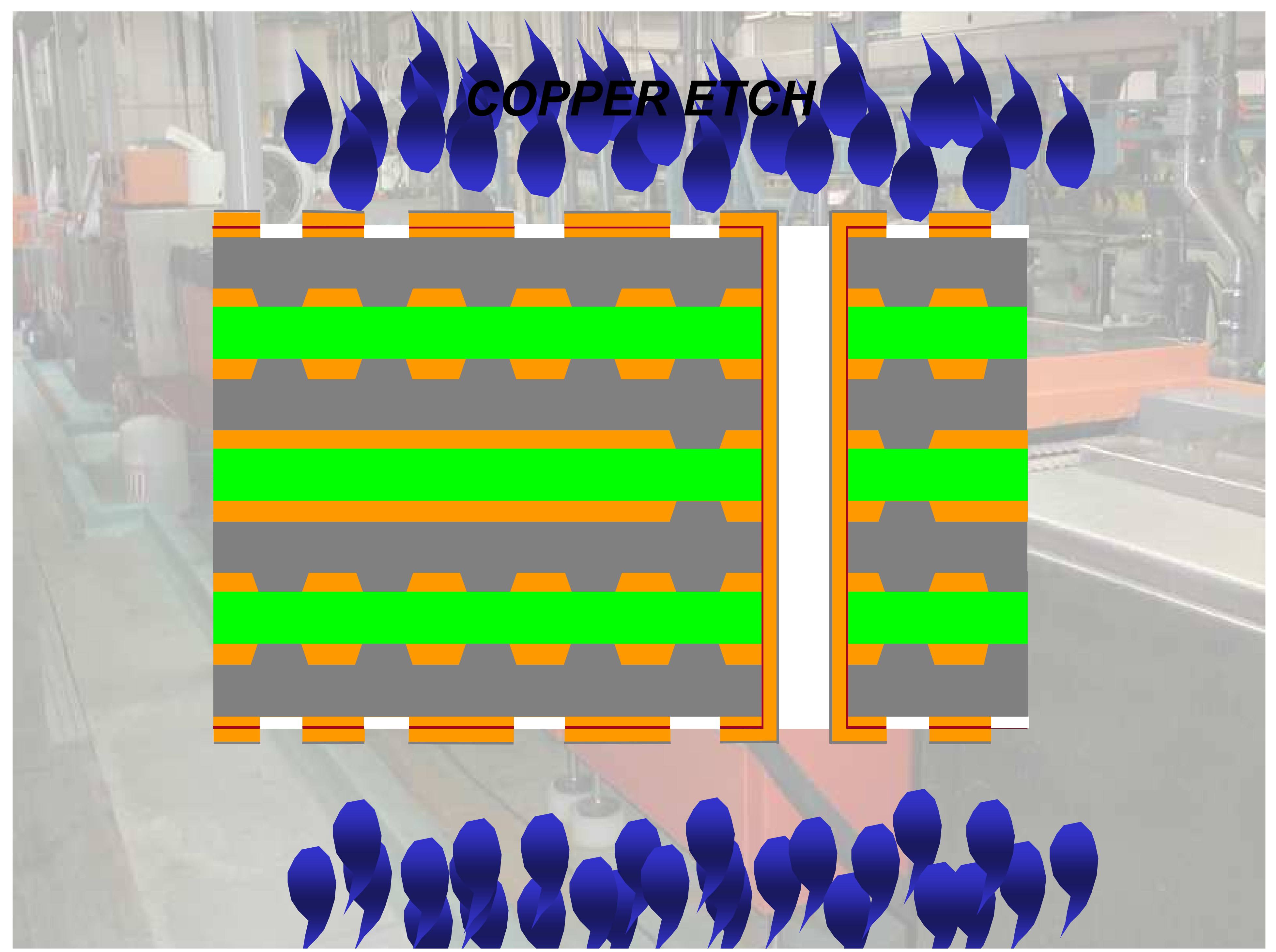

DEVELOP

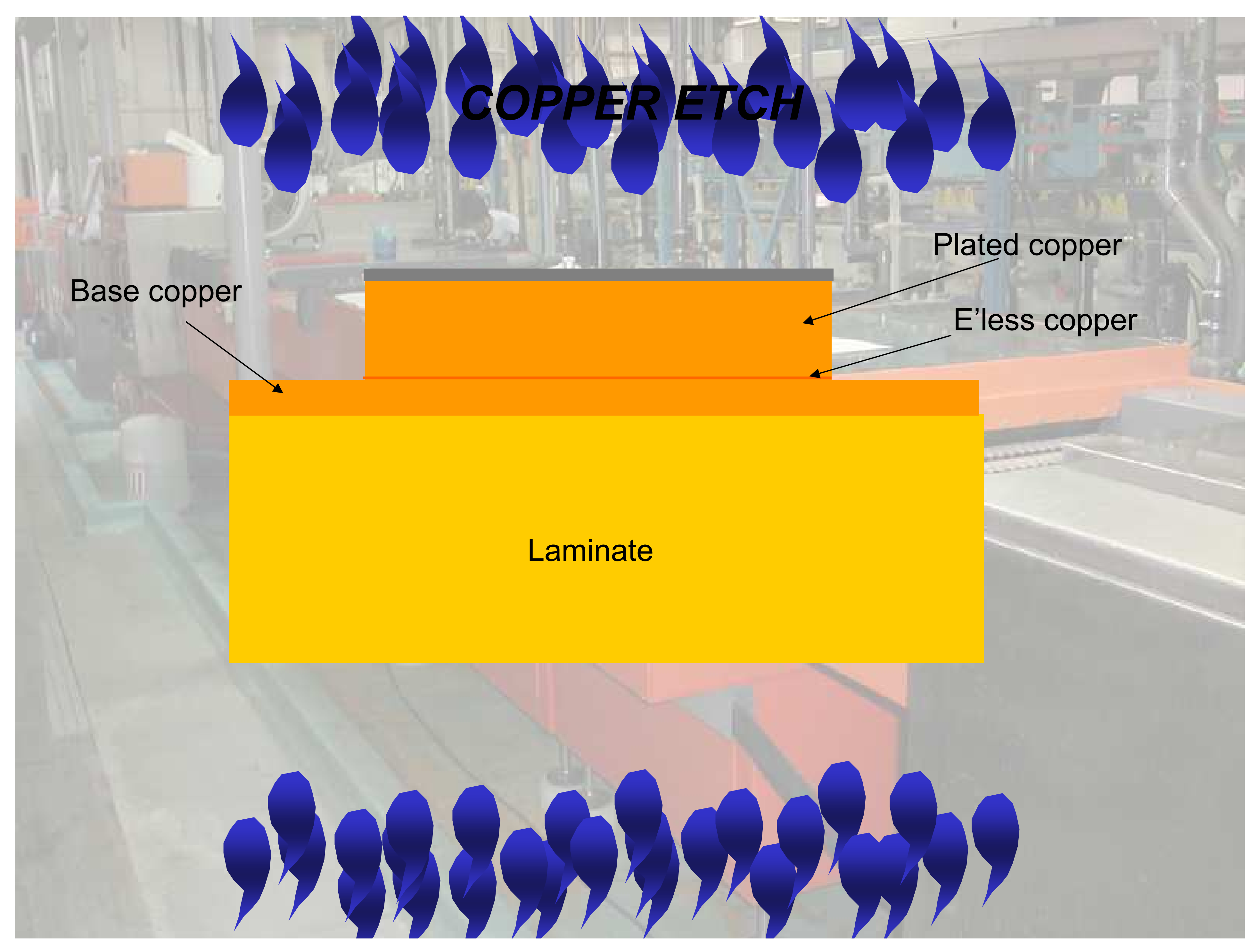
ELECTROLYTIC COPPER PLATE

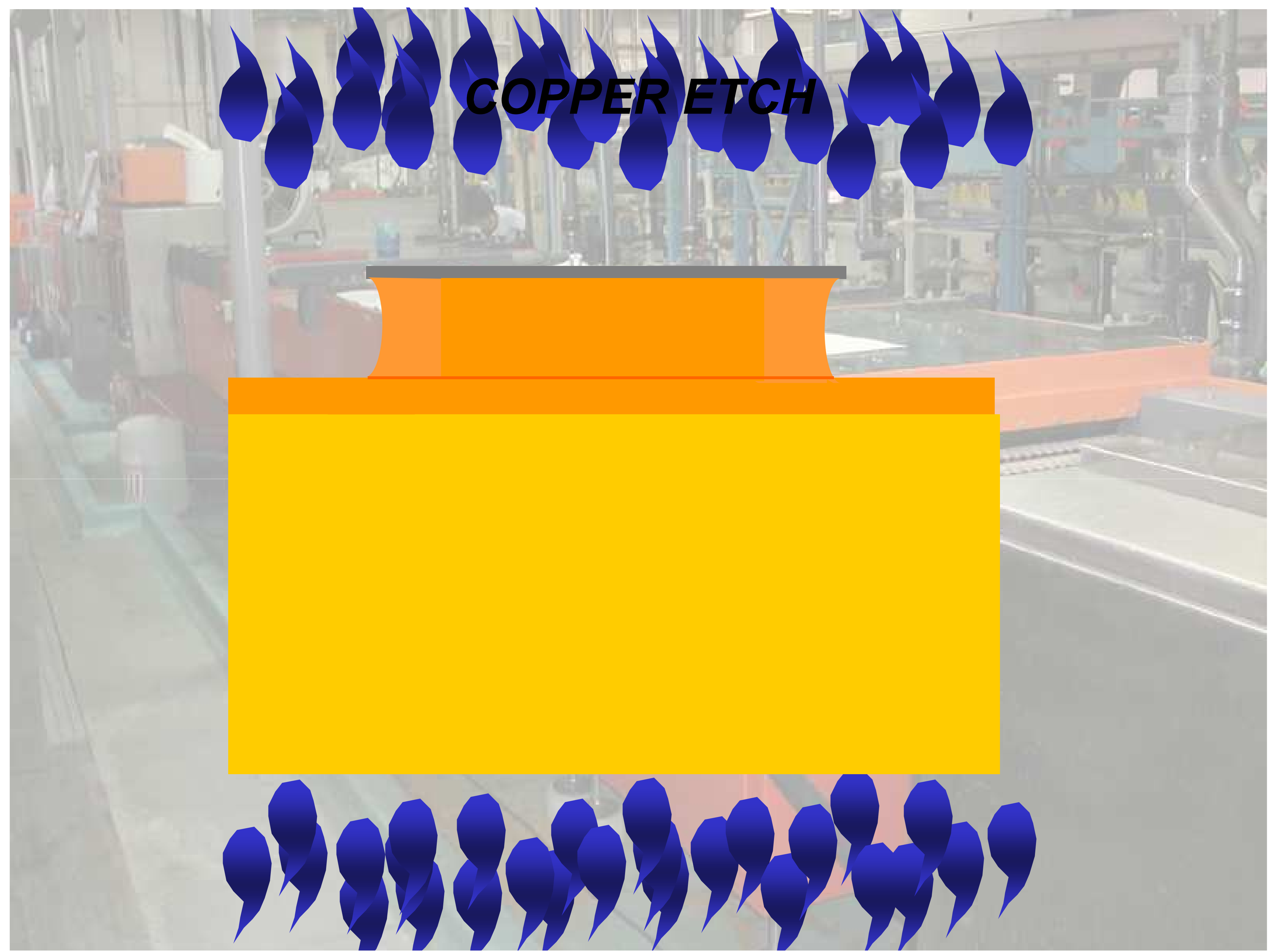

ELECTROLYTIC COPPER PLATE

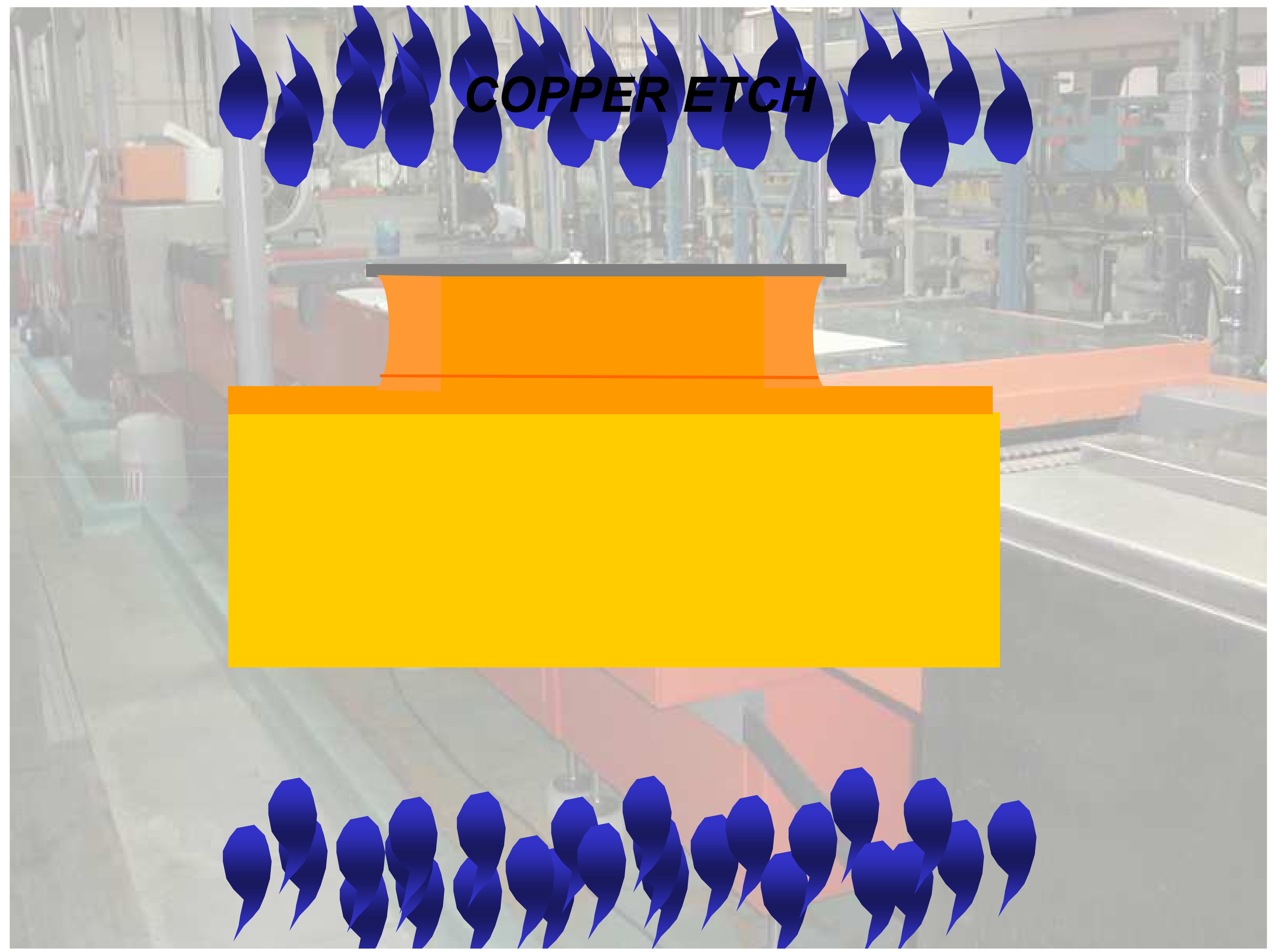

TEMPORARY TIN PLATE (ETCH RESIST)

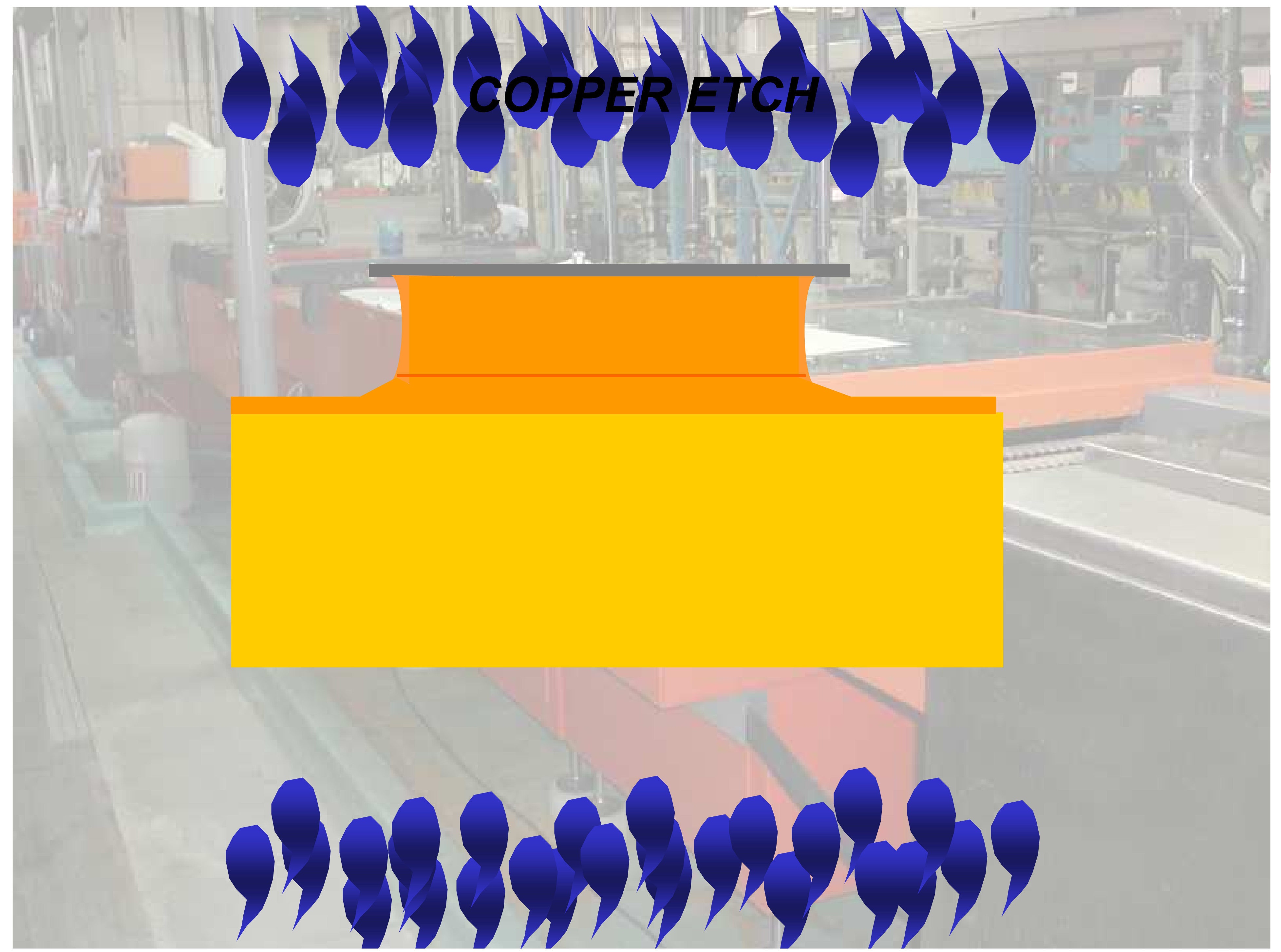

STRIP PHOTO RESIST

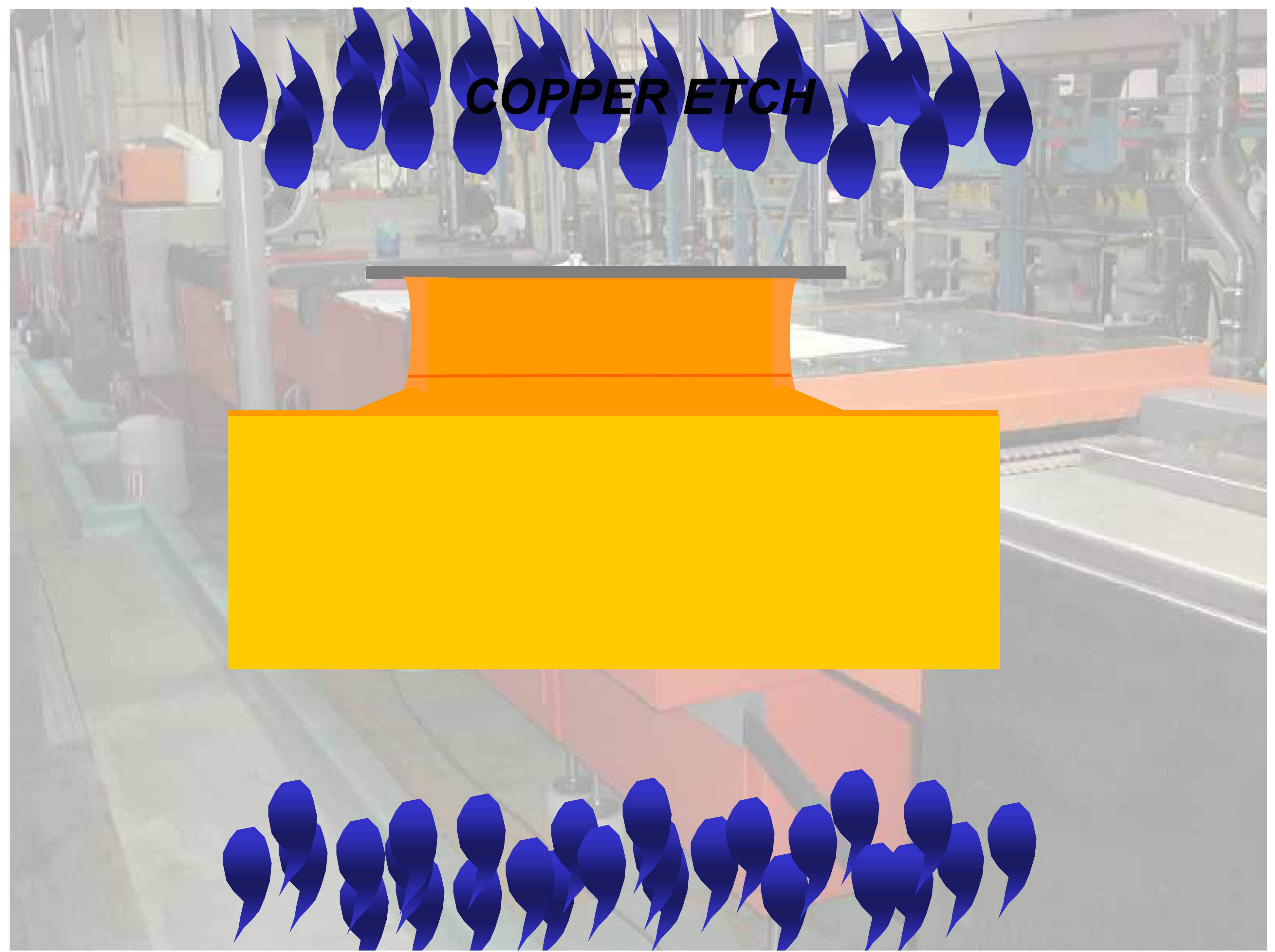

COPPER ETCH

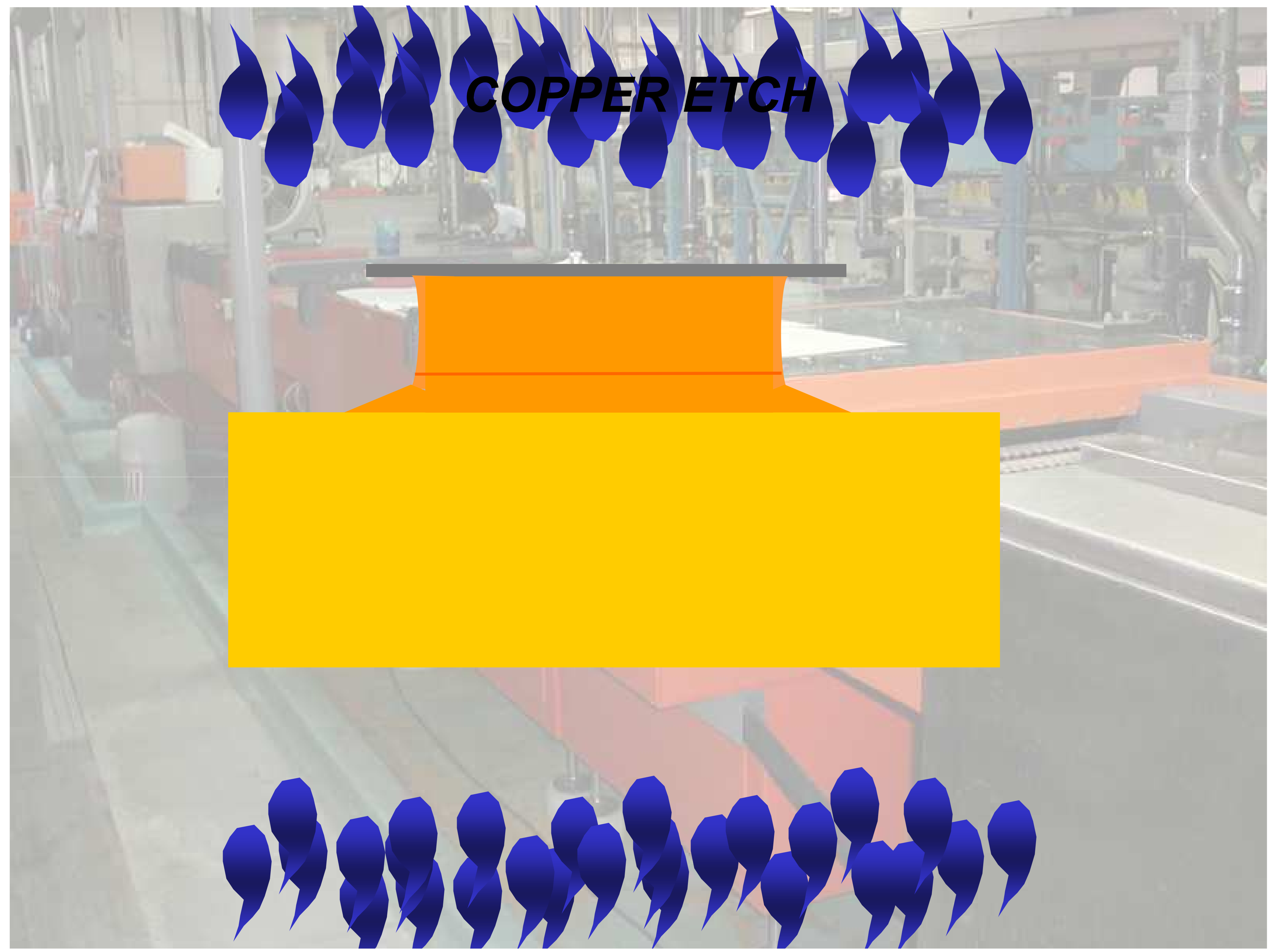

COPPER ETCH
Plated copper
Base copper
E'less copper
Laminate


COPPER ETCH

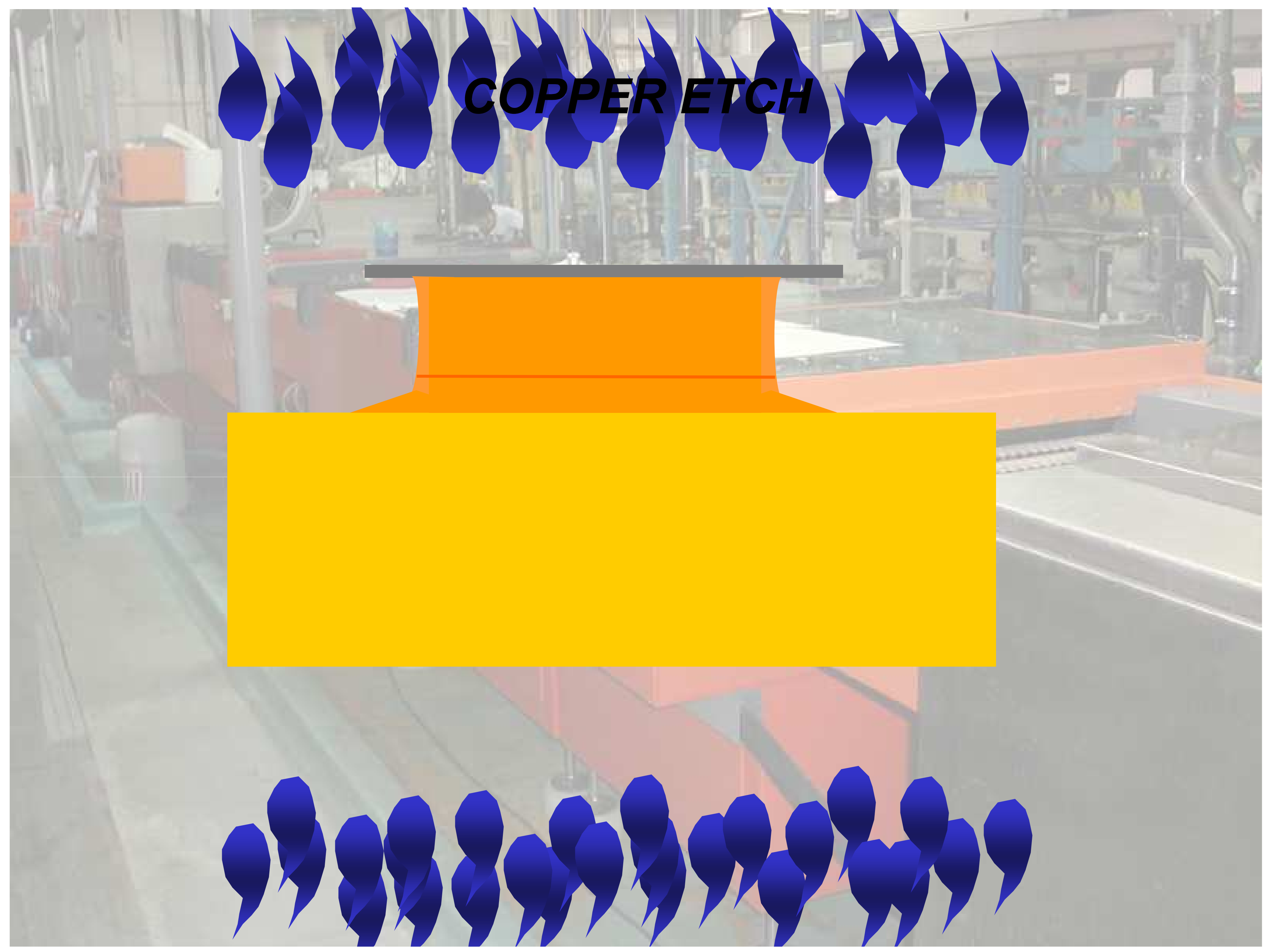

COPPER ETCH

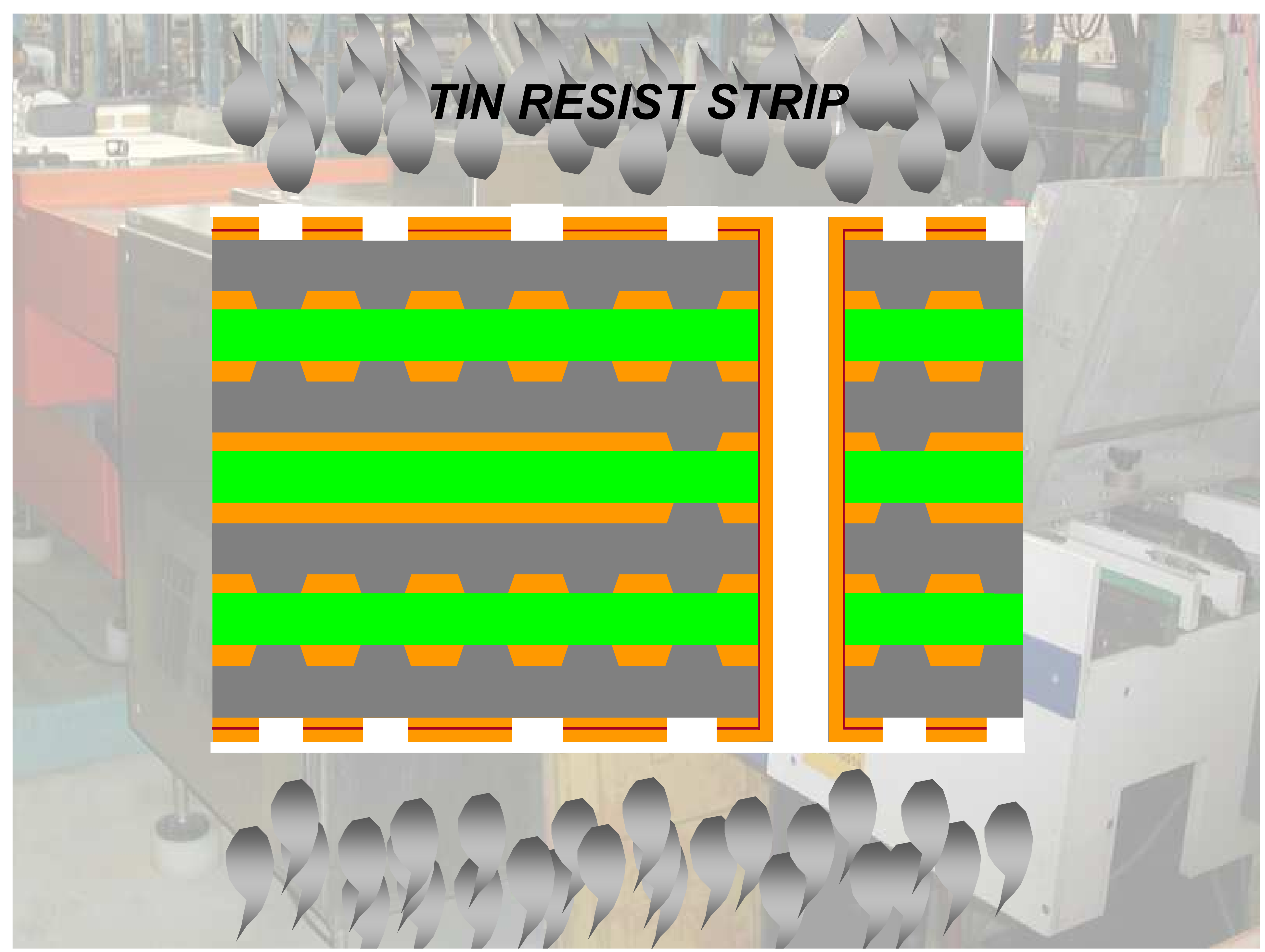

COPPER ETCH


COPPER ETCH

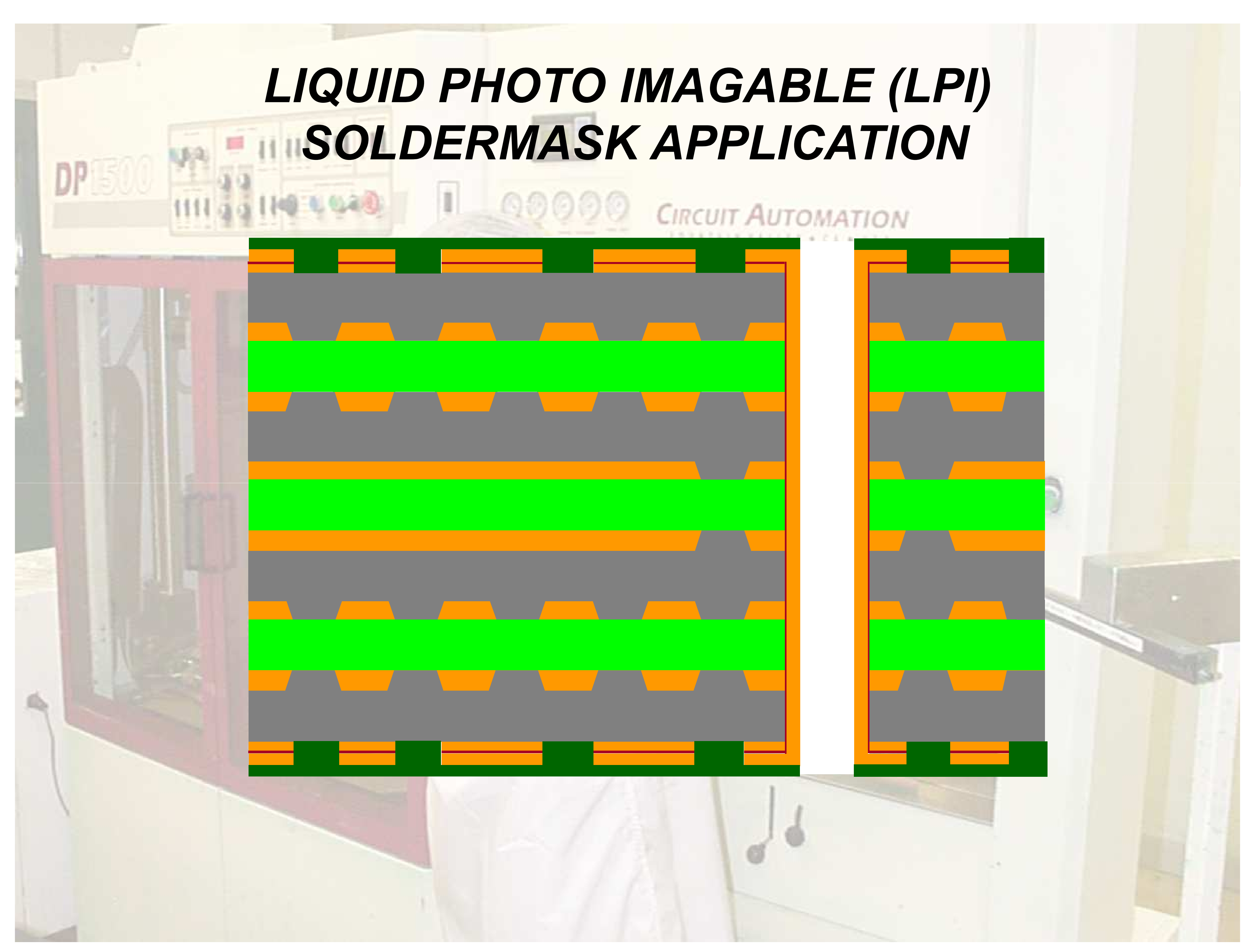


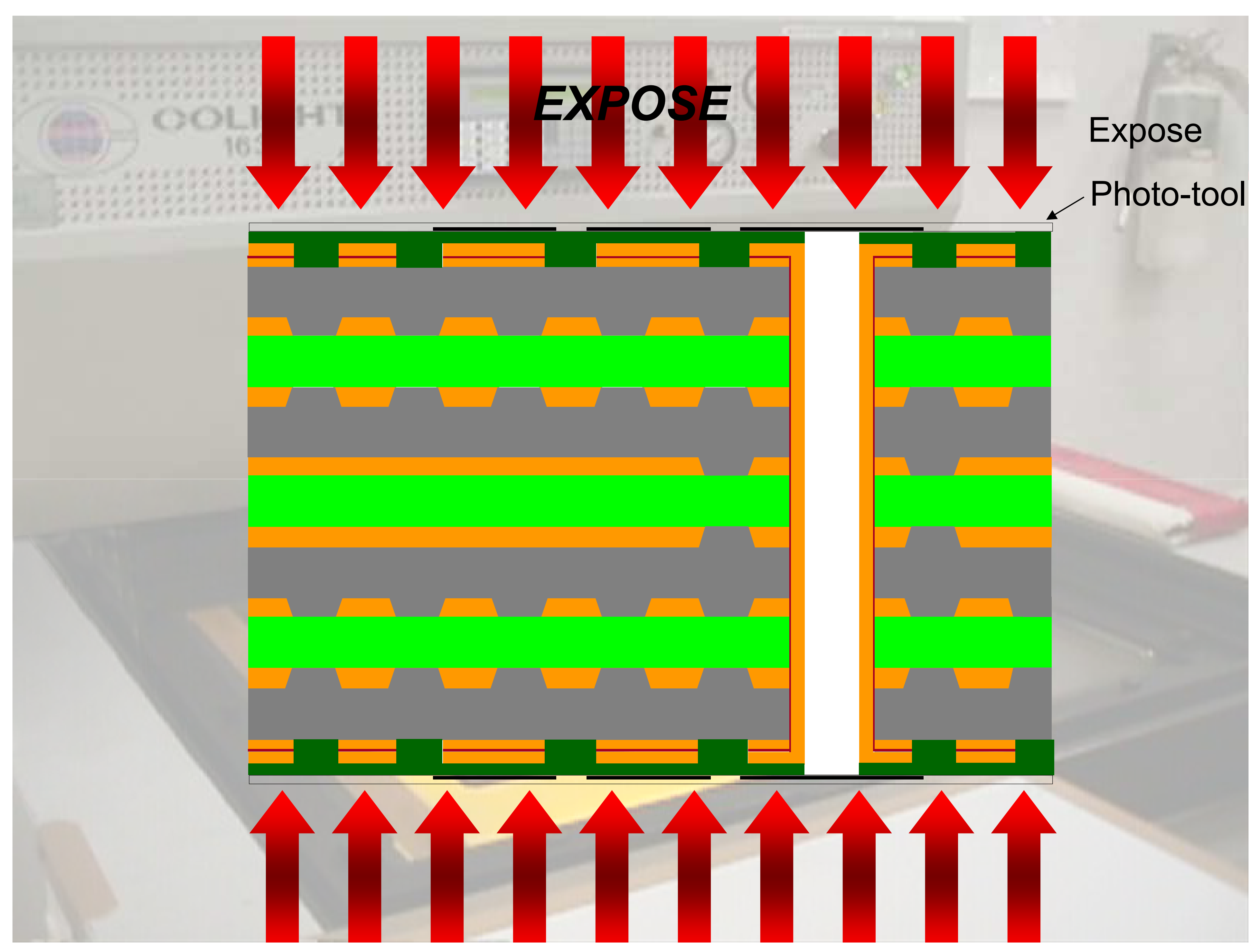
COPPER ETCH

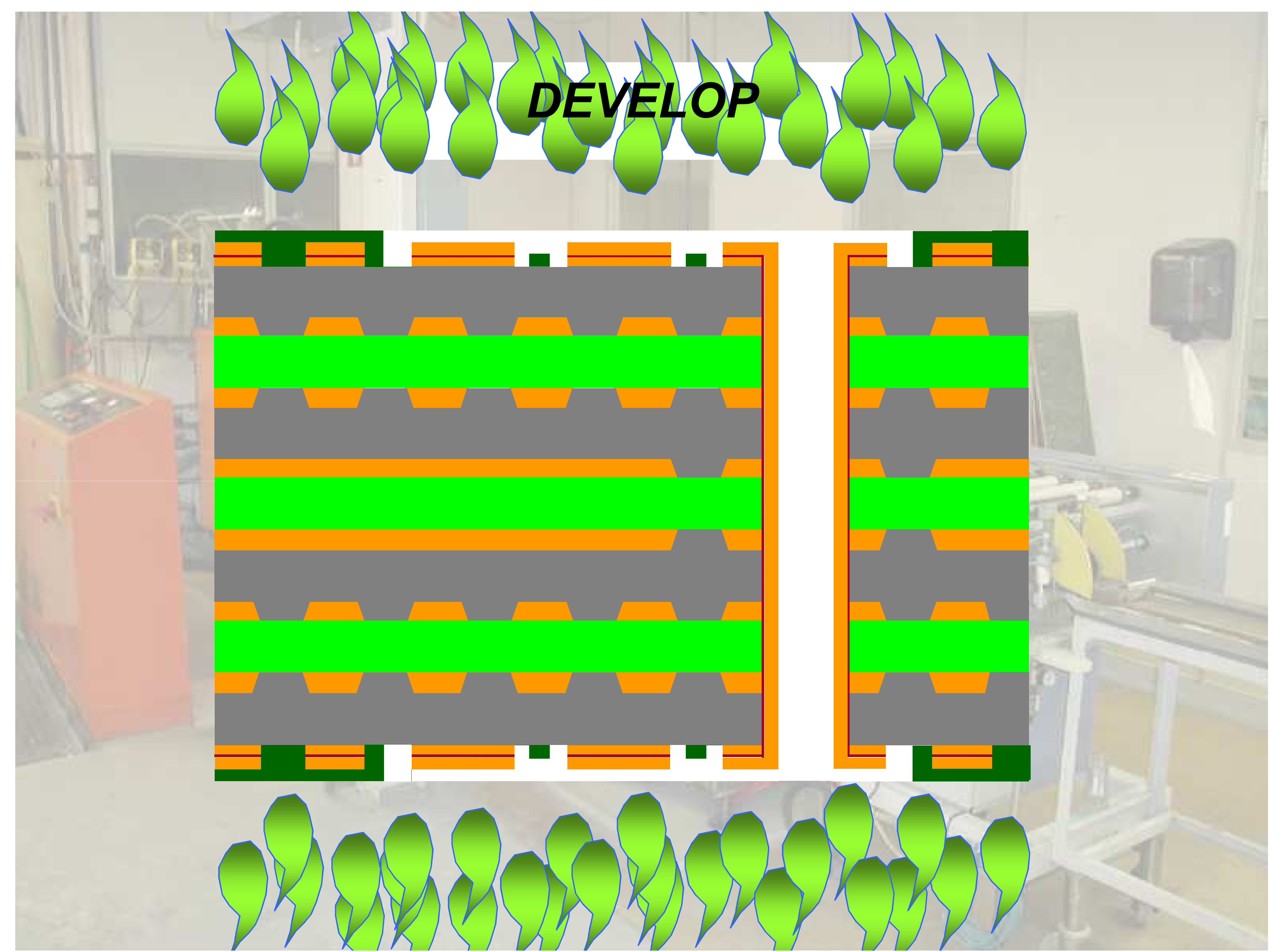

COPPER ETCH


TIN RESIST STRIP

LIQUID PHOTO IMAGABLE (LPI) SOLDERMASK APPLICATION

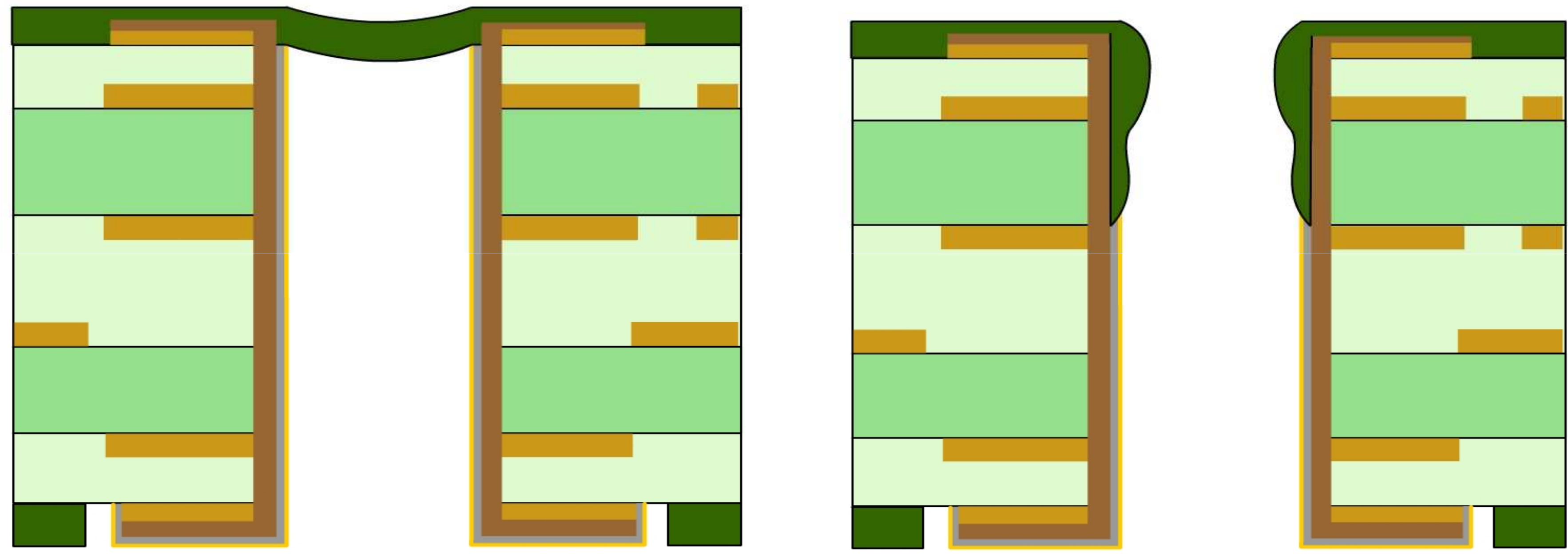



EXPOSE
Expose
Photo-tool

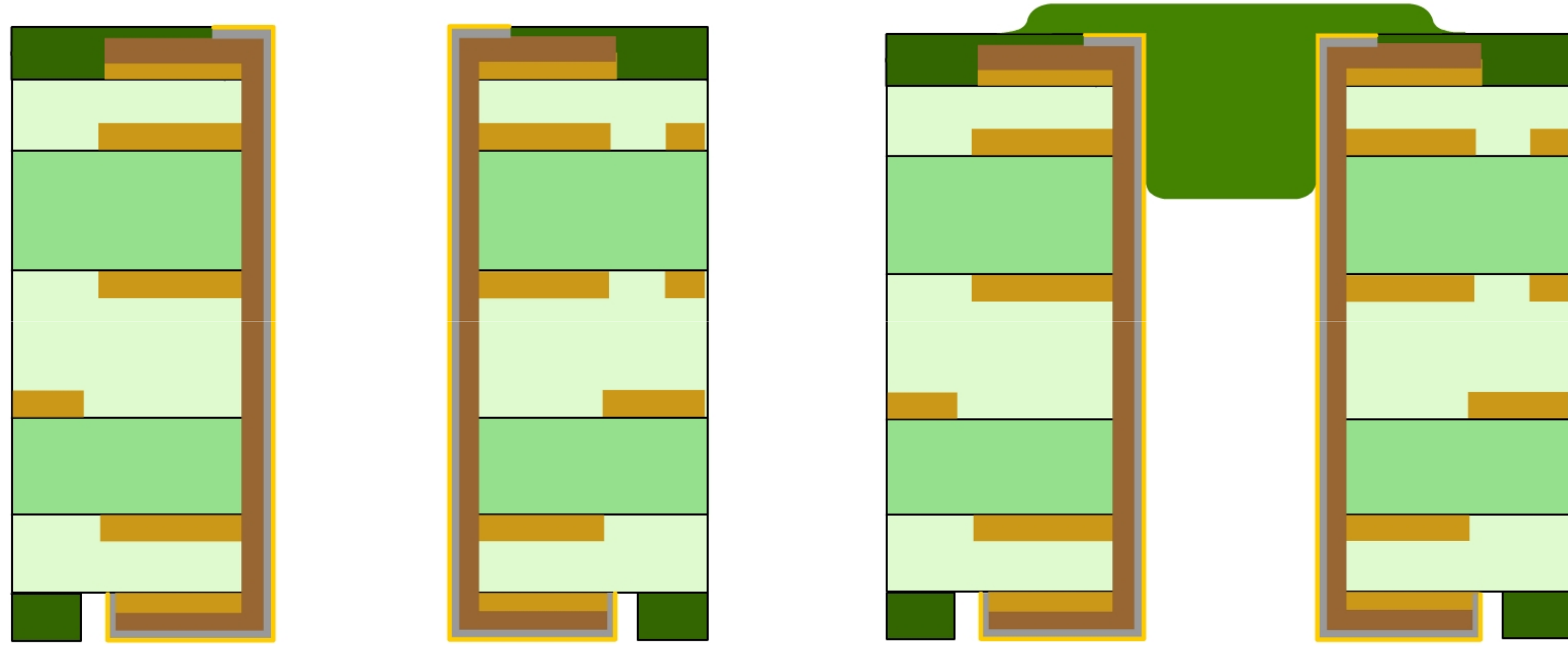

DEVELOP

SOLDERMASK DEVELOP
85
LPI DEVELOPER

SOLDERMASK TENTING

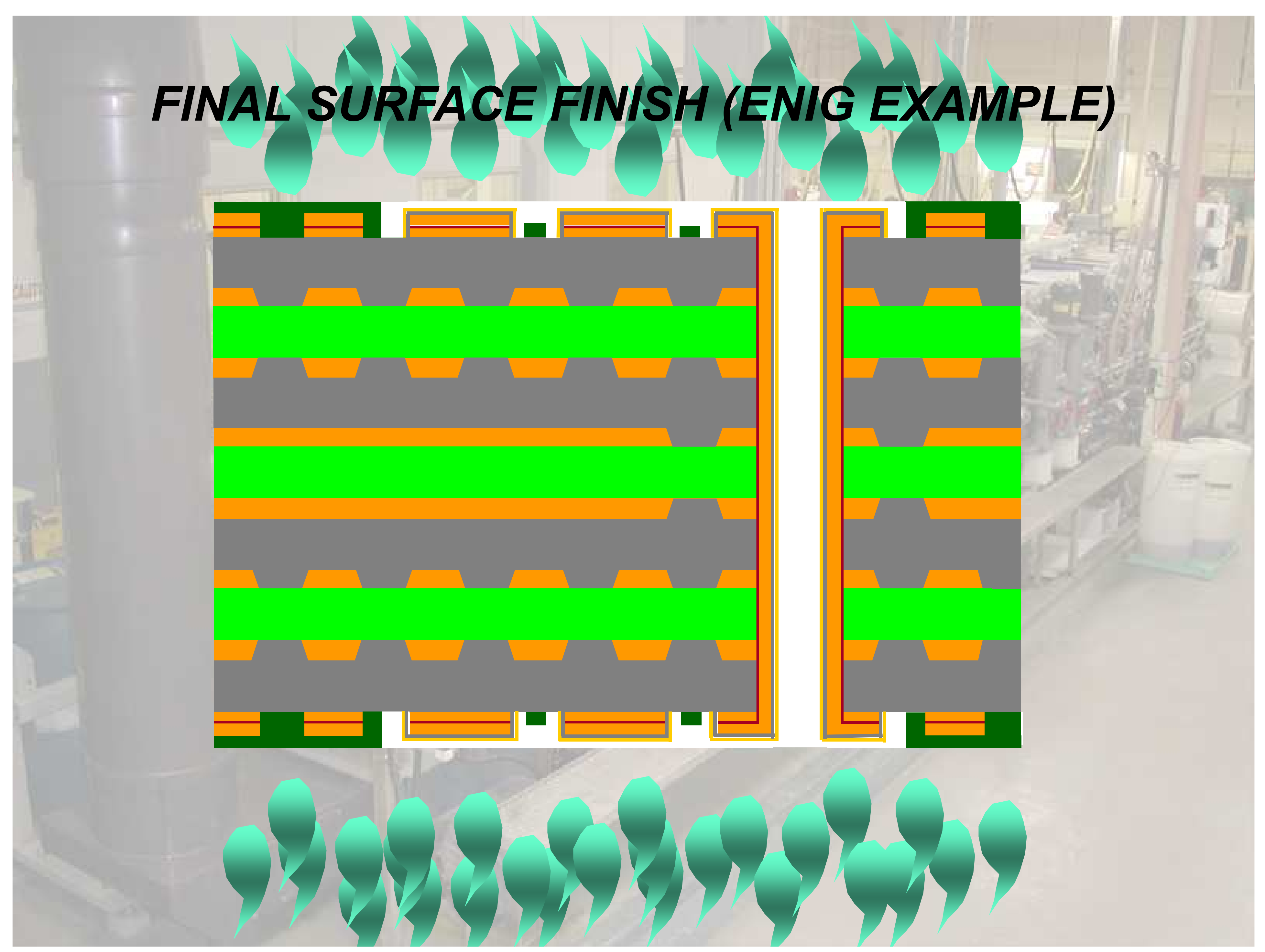


SOLDERMASK TENTING



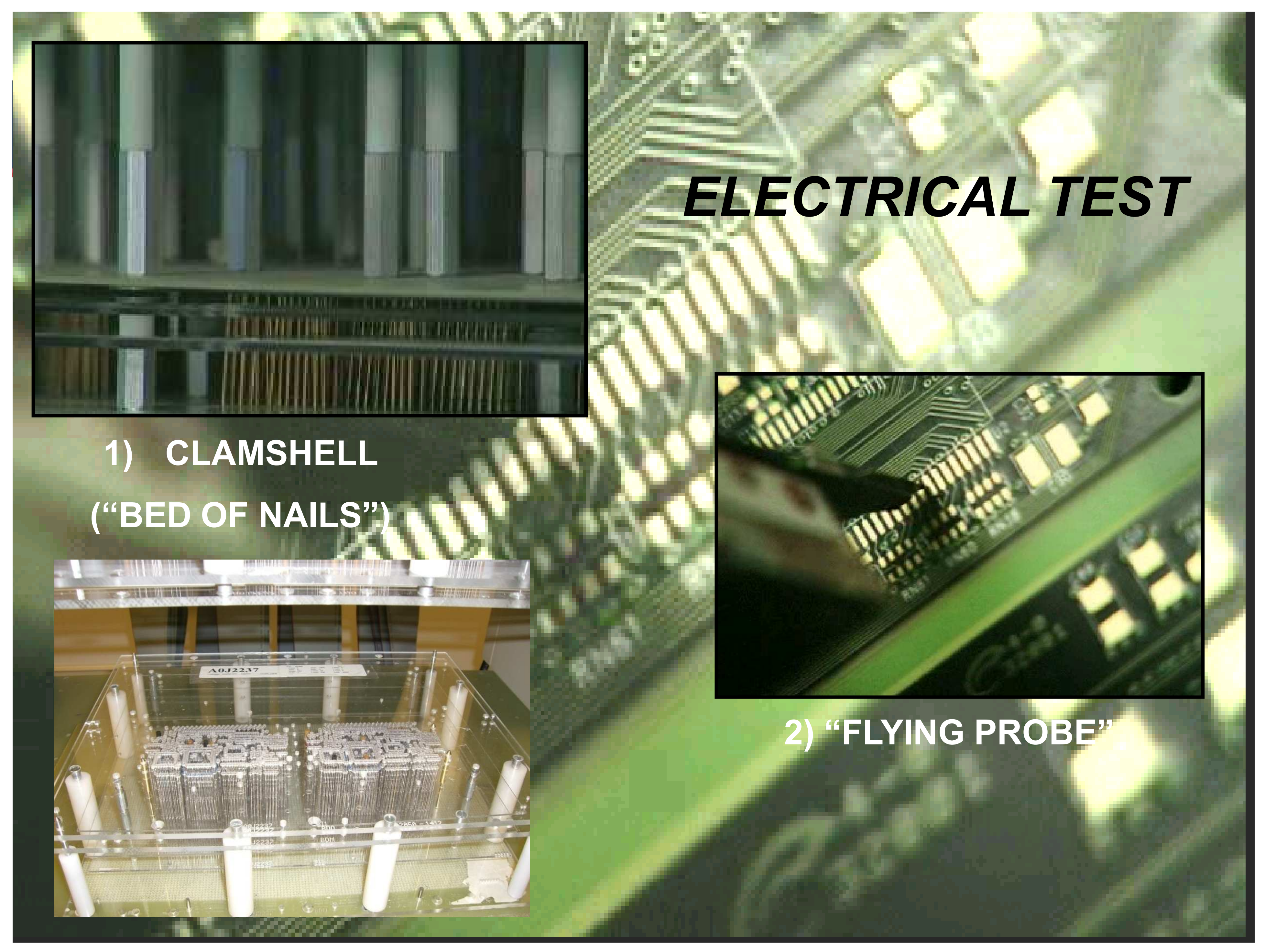
Clearanced (“Encroached”)

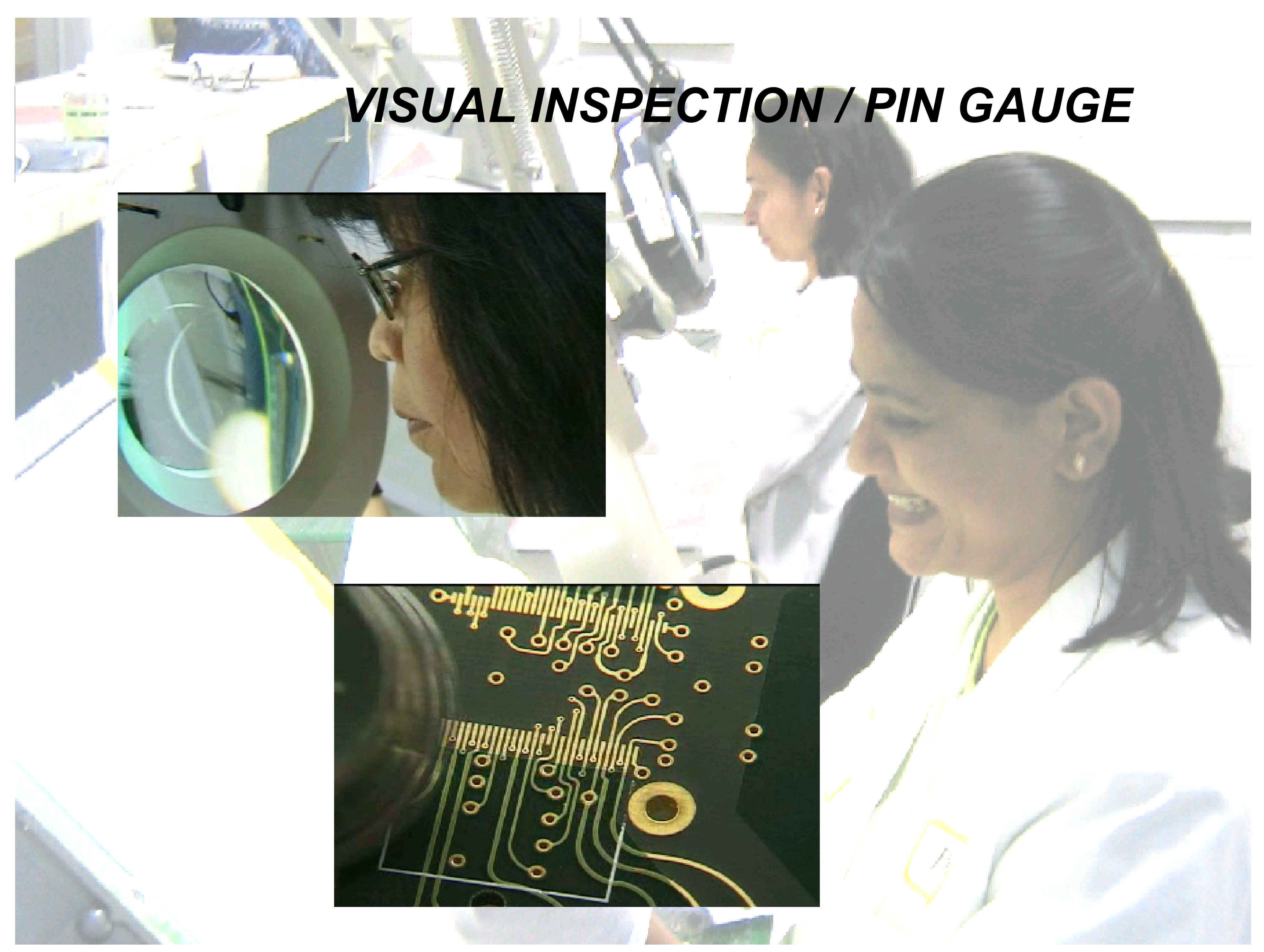
“Tented”


FINAL SURFACE FINISH (ENIG EXAMPLE)

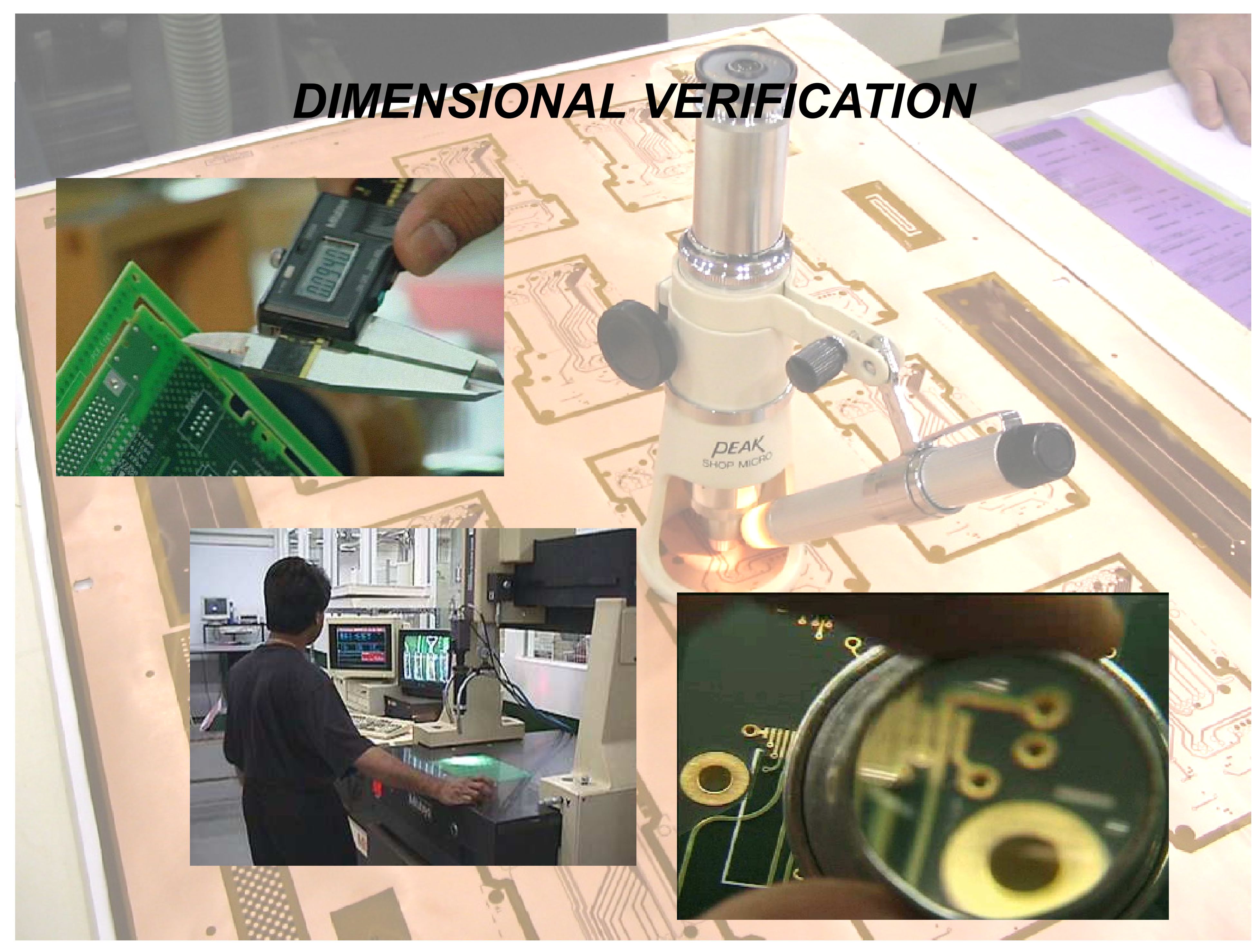
SILKSCREEN NOMENCLATURE

AUTO ROUT (DEPANELIZATION)


ELECTRICAL TEST
1) CLAMSHELL
("BED OF NAILS")
A0J2237
2) "FLYING PROBE"

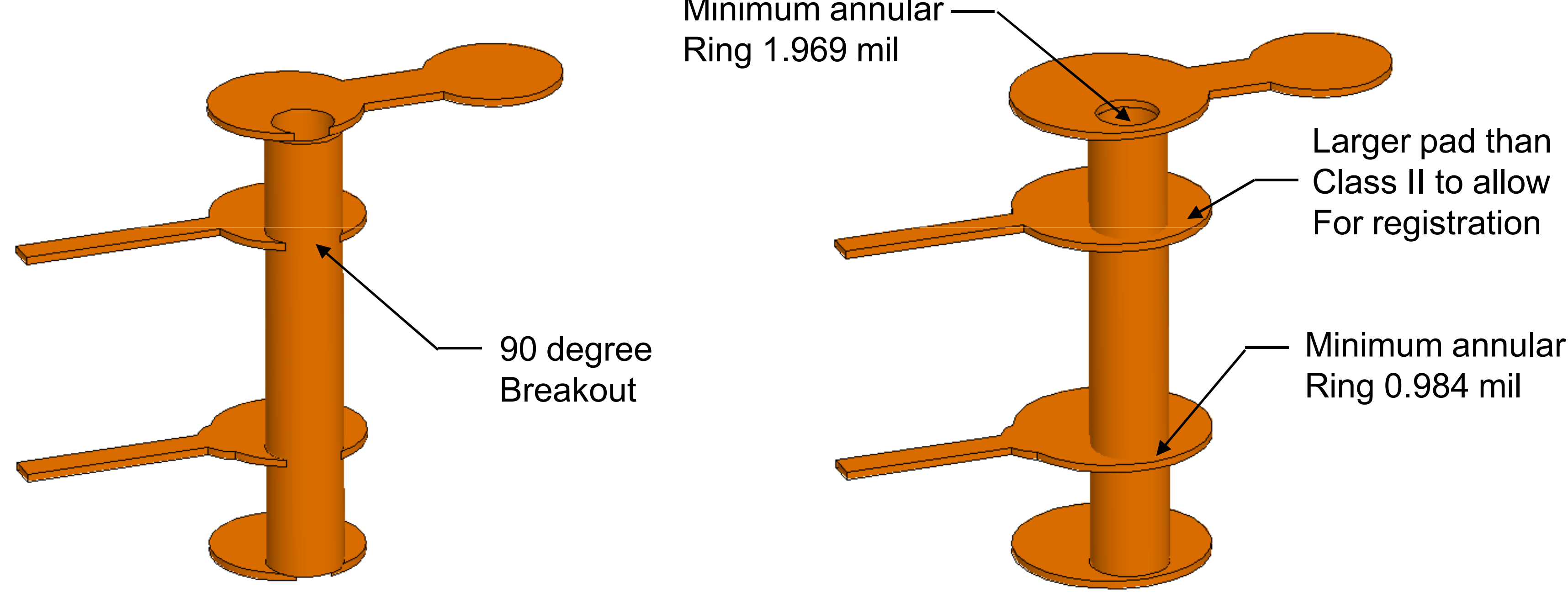

VISUAL INSPECTION / PIN GAUGE

DIMENSIONAL VERIFICATION



MICROSECTION
dy-4,m1-74444-01

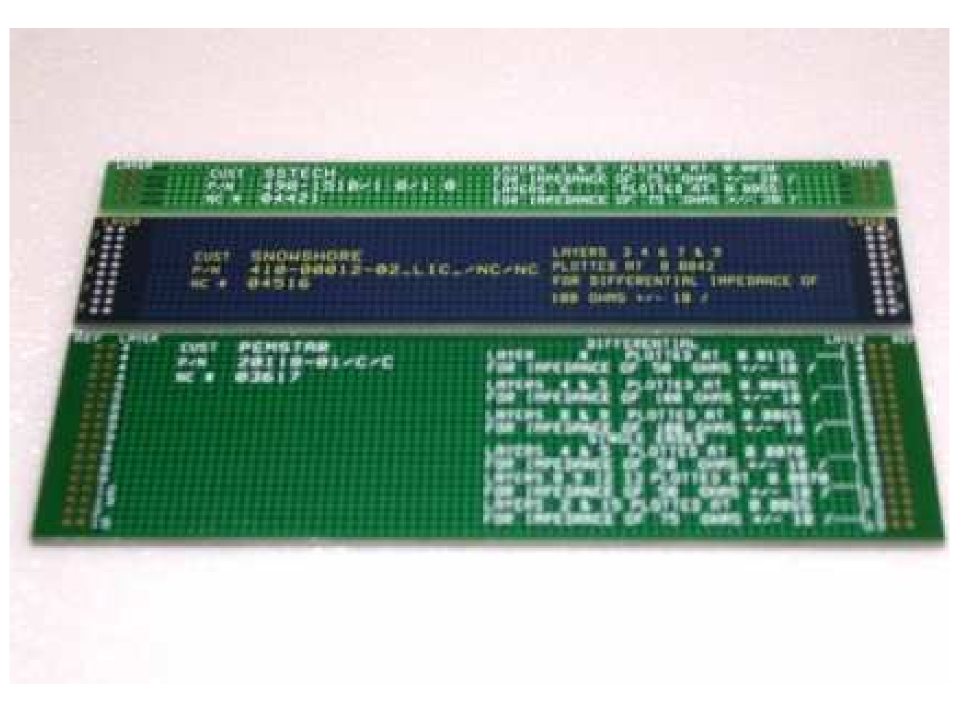
Annular Ring



Worst case registration allowed by IPC Class II

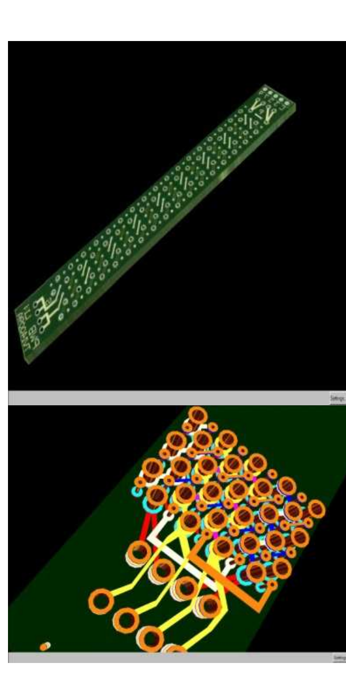
Worst case registration allowed by IPC Class III

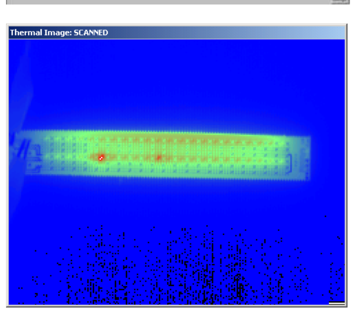
TDR (Impedance Verification)

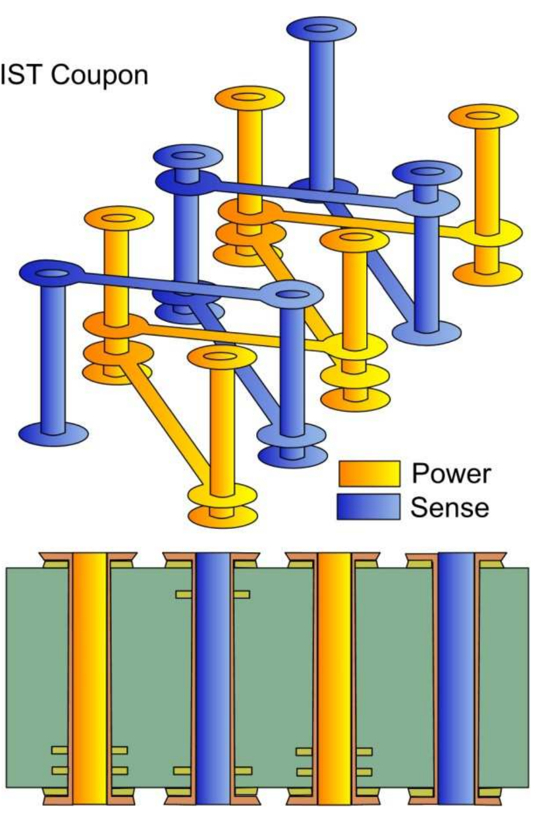


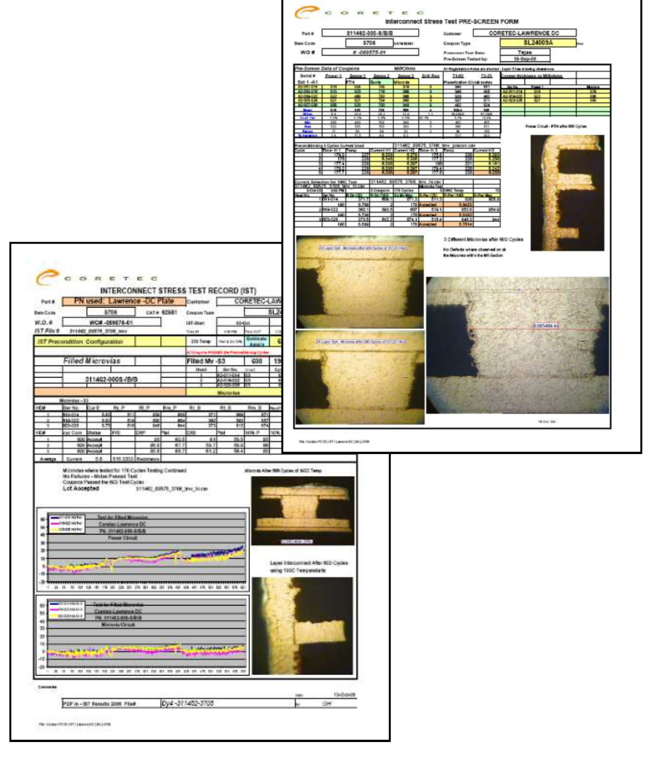
Interconnect Stress Test (IST)

Developed by PWB Interconnect Solutions Inc. (www.pwbcorp.com)









PACK & SHIP

QUESTIONS?

THANK YOU

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Midwest Region
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